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Top-down and bottom-up approaches for SiNWs based micro-TEGs

Outline

- Why «all silicon» TEGs
- Demo applications
- Redundancy
- Thermoelectric generators:
  - bottom-up
  - top-down

Why microenergy solutions: Replace primary batteries (cost, environmental, deployment flexibility issues) by harvesters + secondary batteries

Why Silicon materials and architectures: tap into the micro-nanoelectronics field which is an enabling technology, dealing with miniaturised and high density features (3D) implementations, offering economy of scale (serve mass markets) and the possibility of integration and addition of control and smartness

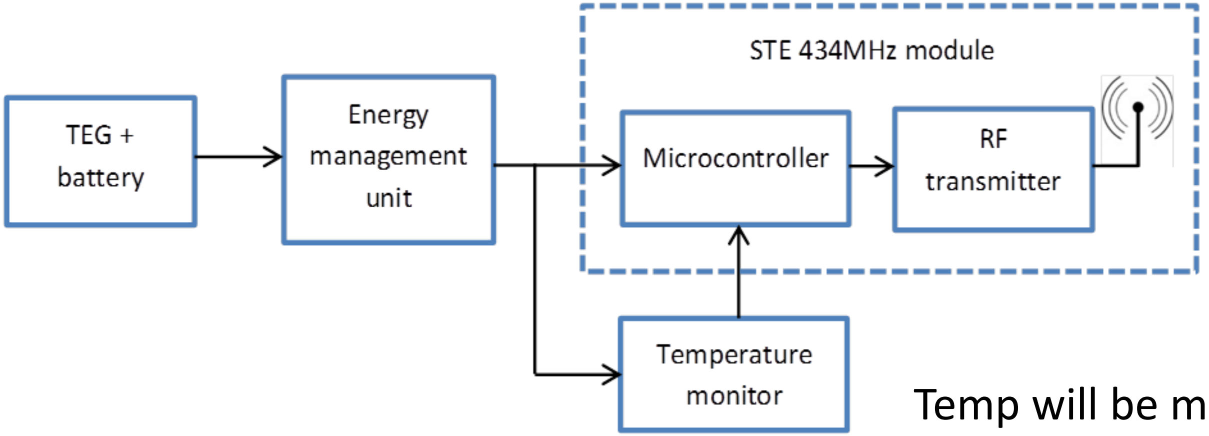
Why such applications: complementary microenergy testbeds from the perspective of silicon benefits ('smaller is better', 'cheaper is better') and availability of energy harvesting sources

Application scenario: Industrial Fryers

Industrial fryers are gas-powered, unplugged industrial appliances.

EC regulations require oil quality to be monitored. A log of oil temperature vs. time would fulfil this obligation.

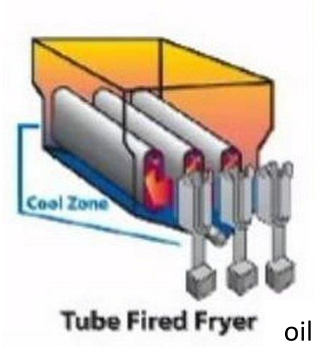
Thermal harvester will supply the power needed to monitor oil temp and to transmit data through a wireless connection to a remote data logging system without the burden of wiring the fryer to the electric net.

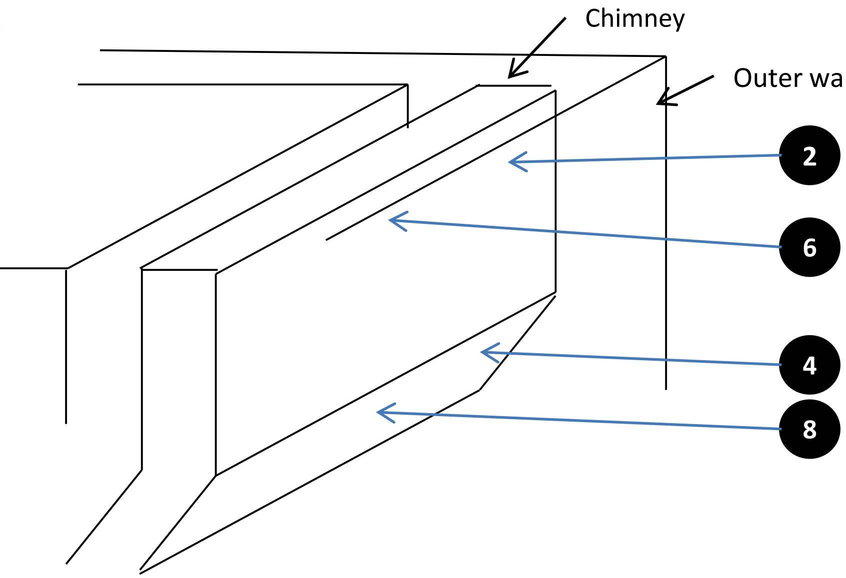


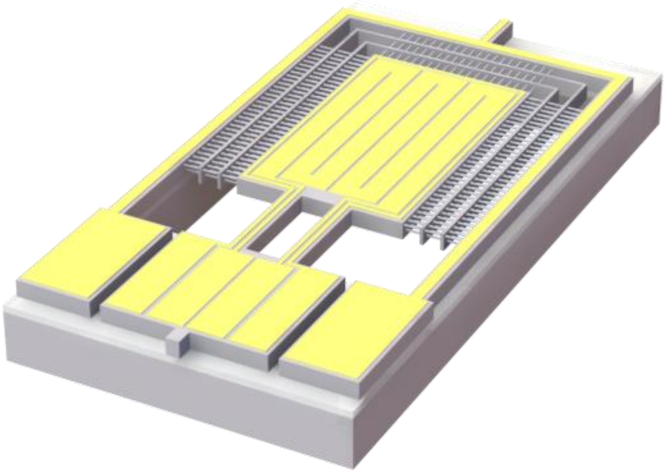
Temp will be monitored using TCs directly connected to the microcontroller

Application scenario: Industrial Fryers

Hot and cold spots needed to thermal harvesters were located at chimney walls.

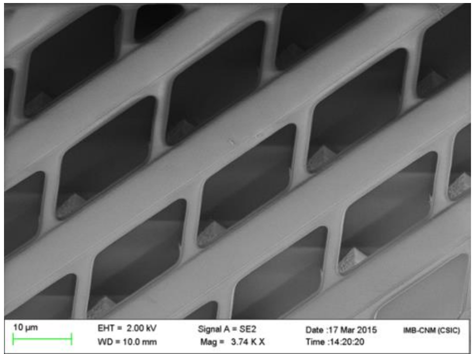






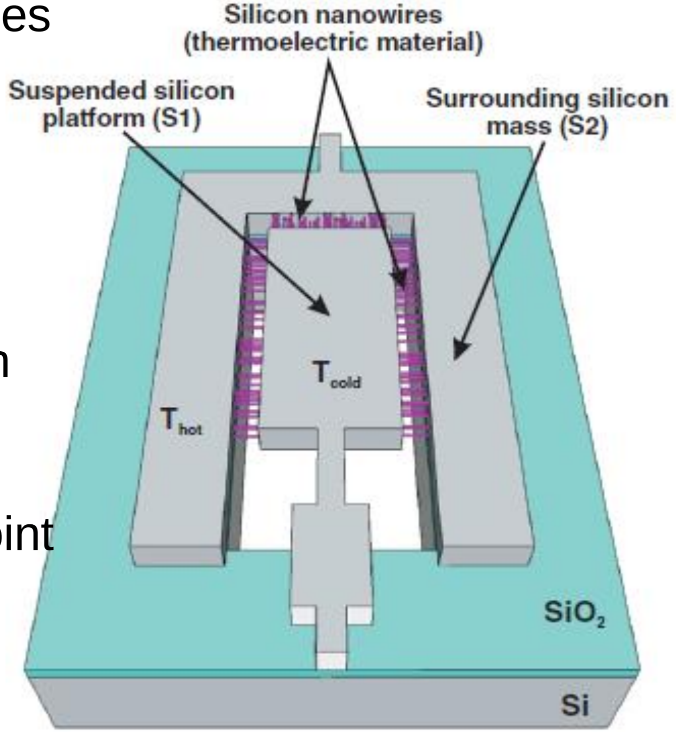
CSIC (Barcelona) and IREC (Barcelona)

THE BOTTOM UP STRATEGY



Bottom-up strategy – The material

- Deposition of gold nanoparticles on device trenches by Galvanic Displacement
- Growth of silicon nanowires on CVD by VLS synthesis
- Removal of membrane and passivation oxide with HF
- Drying of the device with nanowires by Critical Point Drying/Freeze Drying



Dávila et al, J. Elect. Mat., Vol. 40, No. 5, 2011

Microemulsion Galvanic Displacement

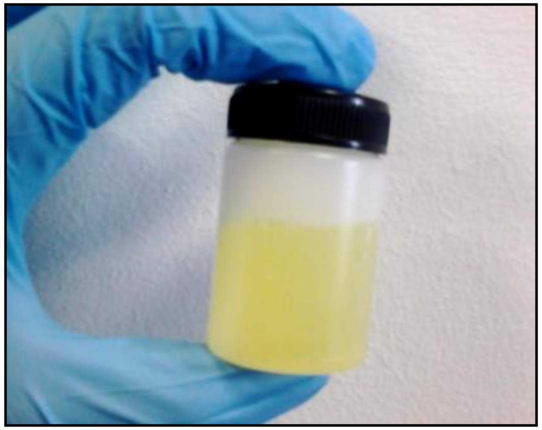
1 – M**icroemulsions** are **prepared**.

Aqueous phase: 0.2M HF + 0.01M $KAuCl_4$

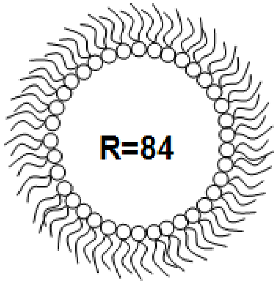
+

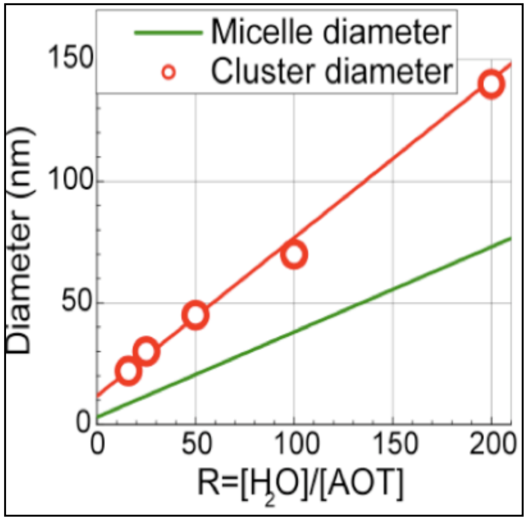
Organic phase: 0.33M AOT (surfactant) in n-heptane

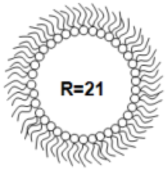
↓

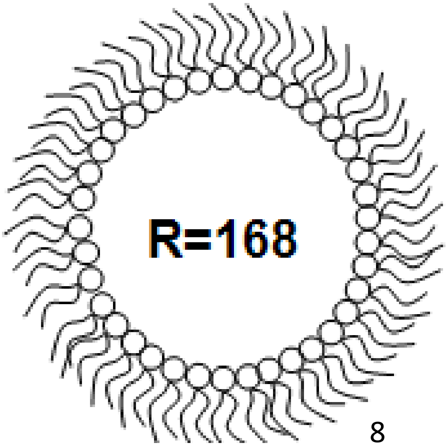


$$R = \frac{[\text{Water}]}{[\text{Surfactant}]} = \frac{[H_2O]}{[AOT]}$$









Gao et al, J. Am. Chem. Soc. 127, 4574 (2005)

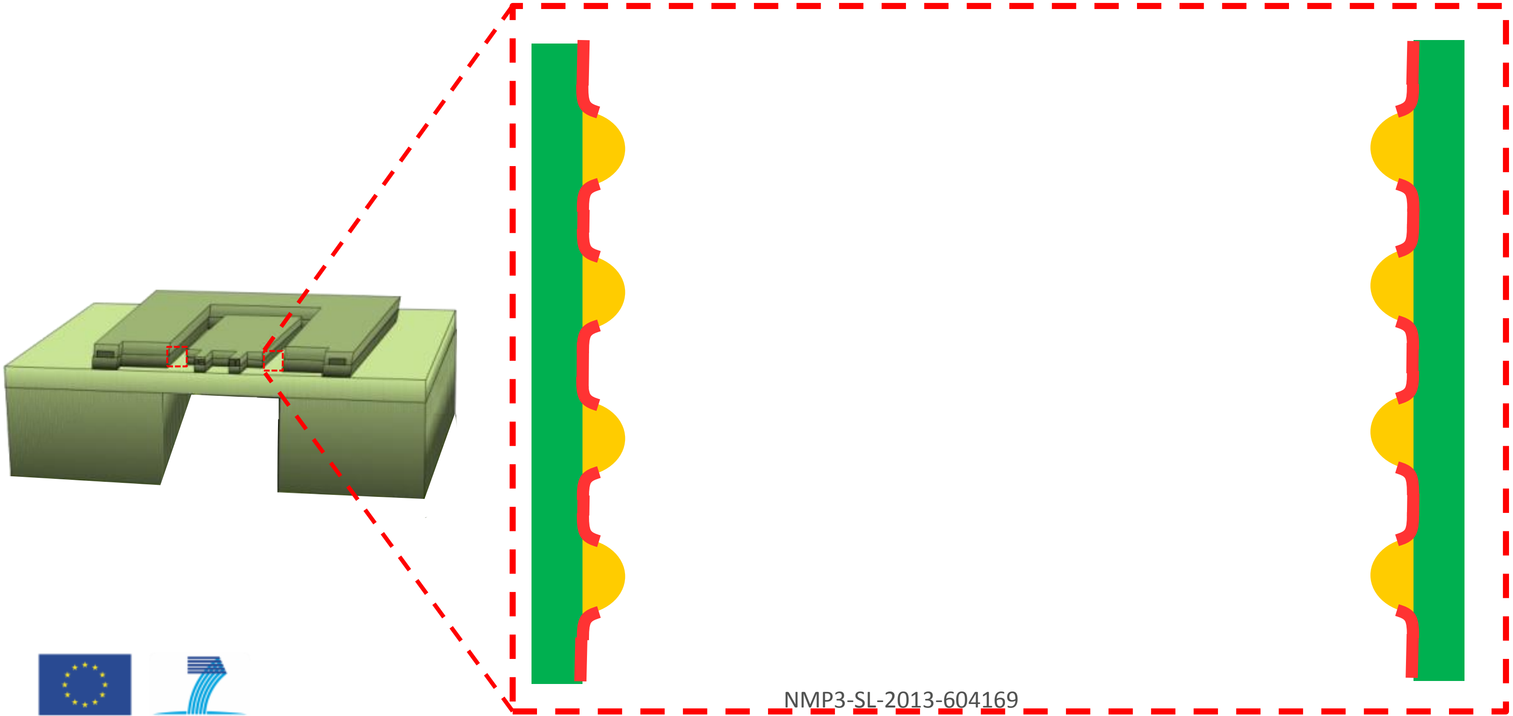
Microemulsion Galvanic Displacement

1 – Several **microemulsions** with different R values are **prepared**.

2 – Devices are **dipped in HF** in order to remove native oxide from trenches

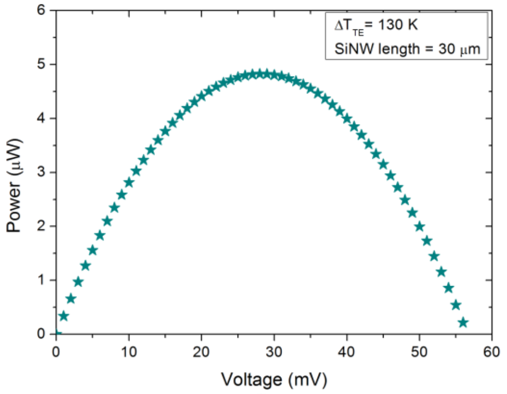
3 – Devices are **dipped in microemulsions** during a controlled dipping time. Gold NPs are formed

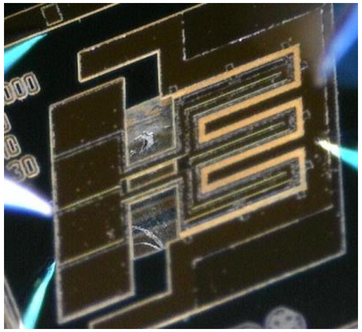
4 – Devices are **annealed** to remove the remaining surfactant



μTEG basic characterization – IV curve

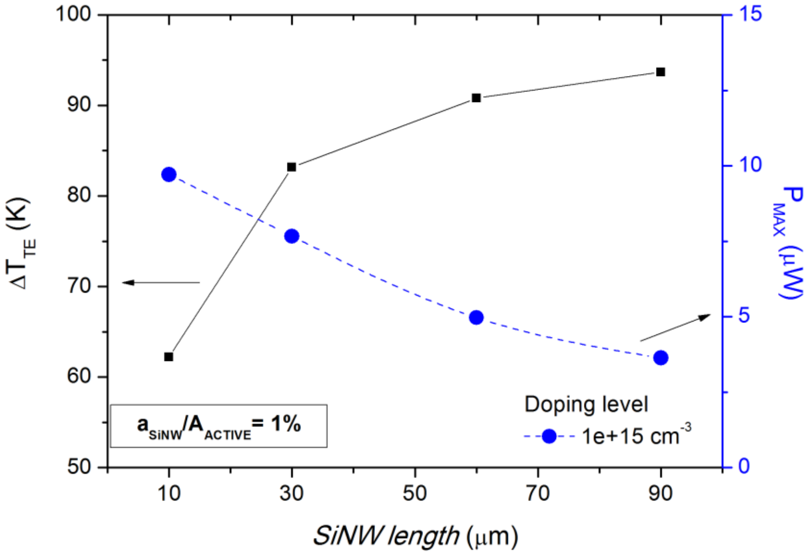
Real device under test mode



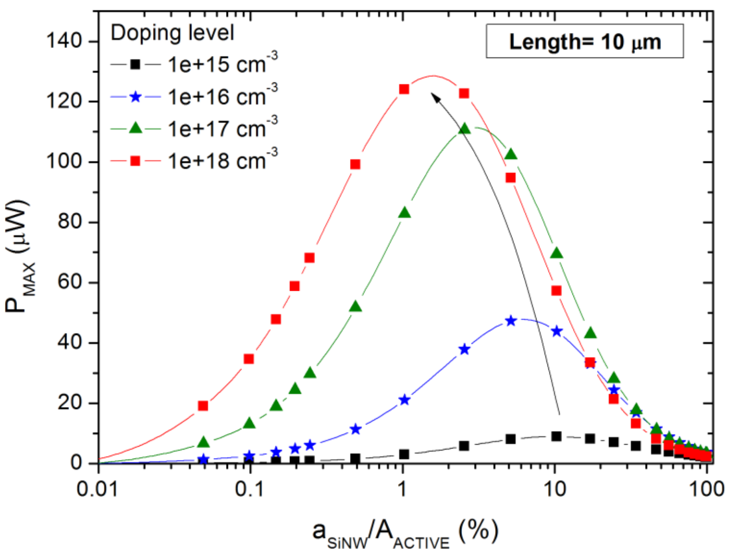


Parameter	Value
S_{SiNW}	*1.46e-3 V/K*
ρ_{SiNW}	*13.5 Ωcm*
k_{SiNW}	*50 W/mK*
L_{SiNW}	*10 - 90 μm*
$r_{AMBIENT}$	*76.4 K/W*
R_{PATH}	*50 Ω*
ΔT_{TE}	*100 K*

Effect of low doping level of SiNW - Non-optimized device



Effect of SiNW doping level - Optimized device

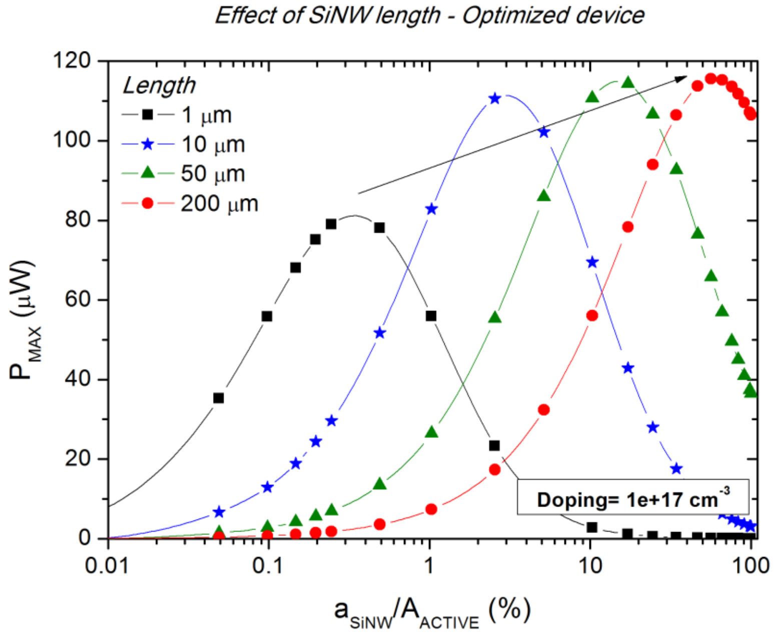


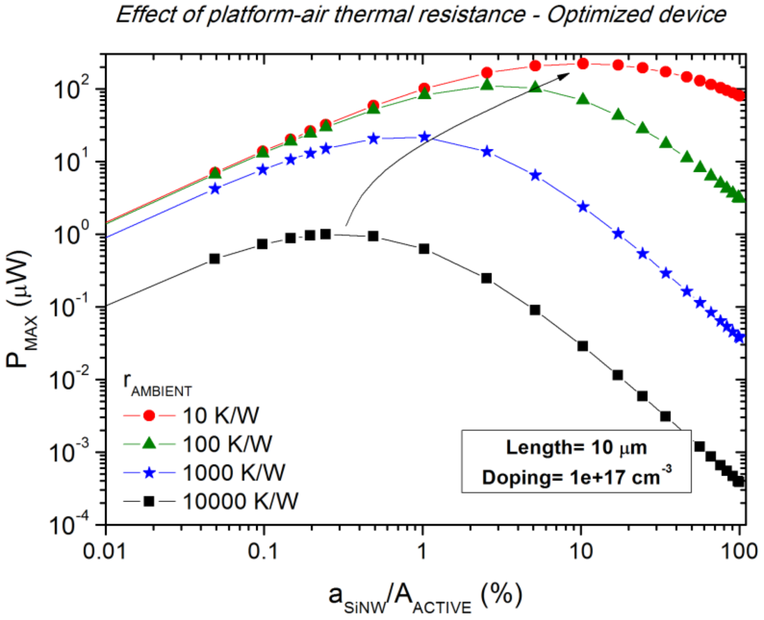
µTEG basic characterization – IV curve

ining the device I-V curve

oping level effect on device performance

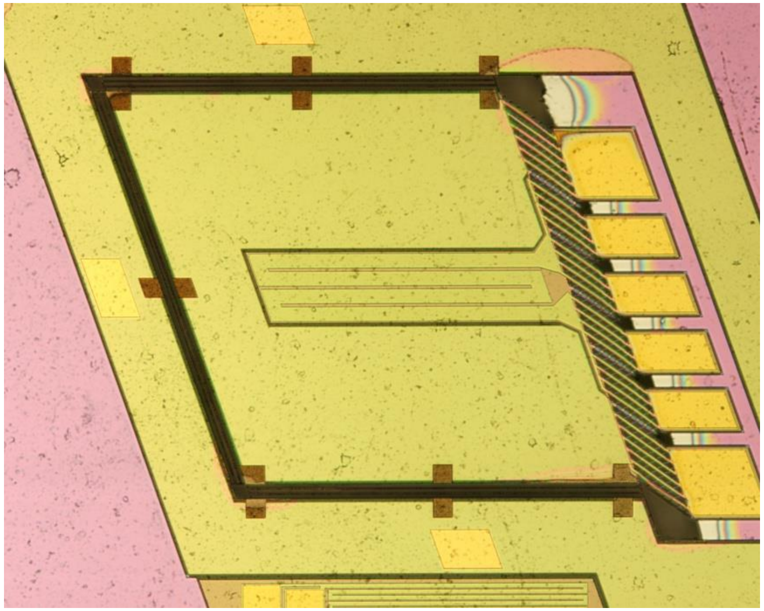
iNW density effect on device performance


Effect of SiNW length - Optimized device


Effect of platform-air thermal resistance - Optimized device

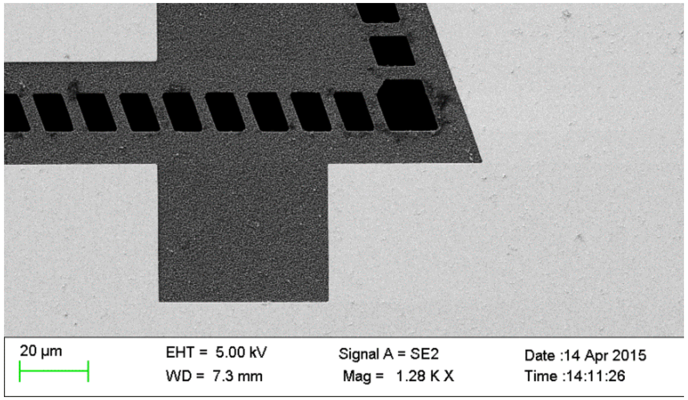
Bottom-up strategy – Si platforms

- Multiple configurations, for pure harvesting or test purposes, with built-in heaters for characterization with controlled gradients.

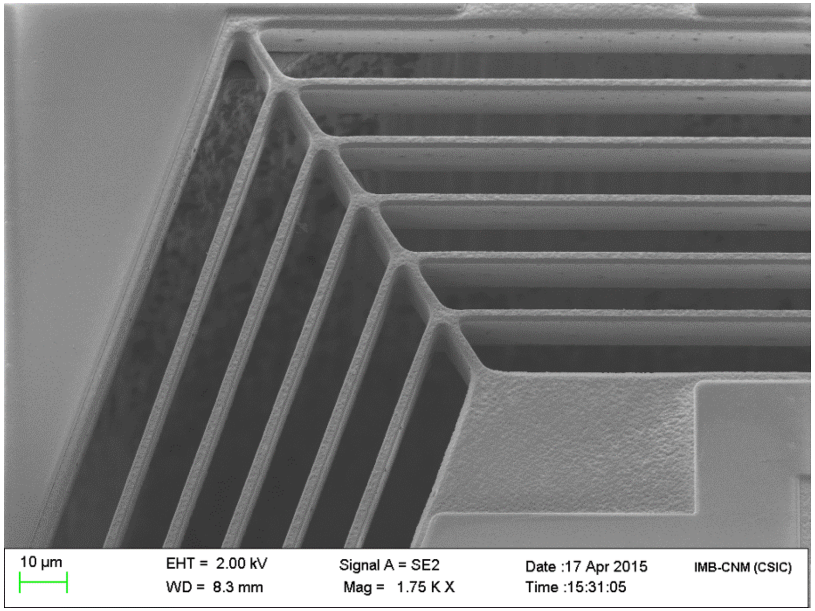


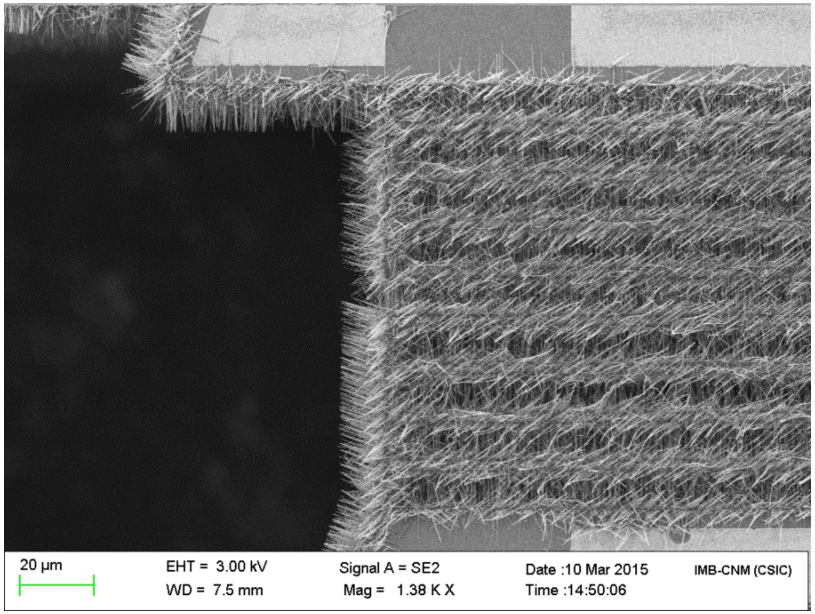
- Series and parallel connections of multiple devices.

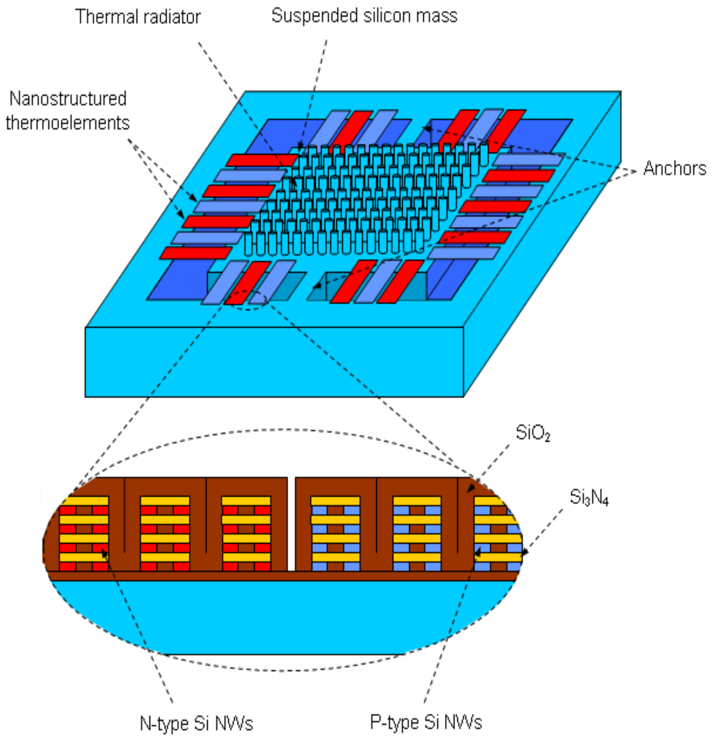
- different length of membranes.
- different numbers of trenches (1 to 4) to be filled by Si NWs.
- bridges in place of membranes.
- no temporary Si bulk supports.
- prefixed percentages of bulk Si.



Bottom-up strategy – Si platforms

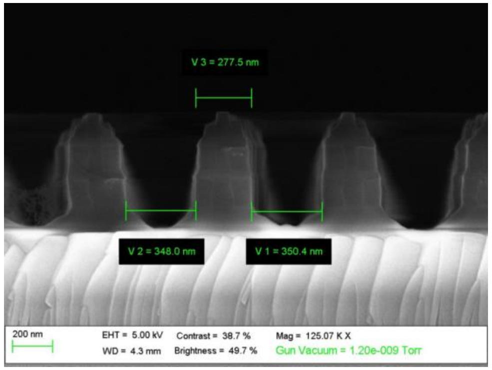






IMM-CNR (Bologna) and Univ. of Milano Bicocca

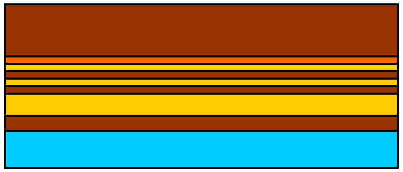
THE TOP-DOWN APPROACH



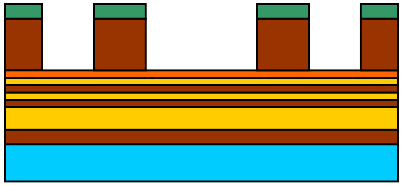
Lateral TEG - process flow (1)

1. Bulk Si

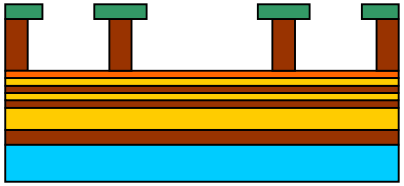
2. SiO_2/Si_3N_4/poly deposition



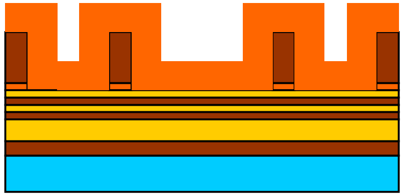
3. SiO_2 RIE



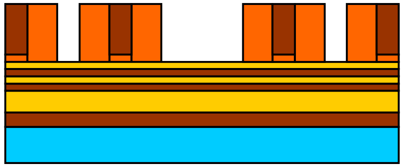
4. SiO_2 wet etching



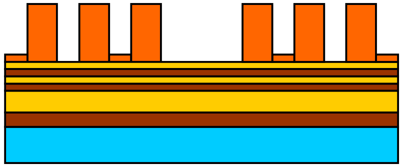
5. Poly deposition



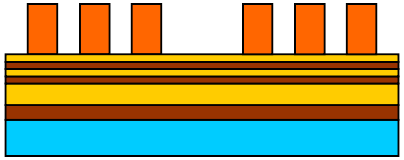
6. Poly RIE



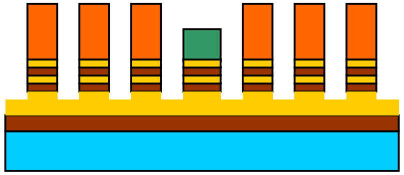
7. SiO_2 wet etching



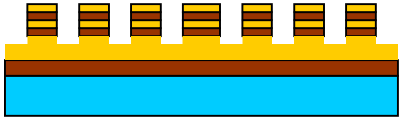
8. Poly RIE



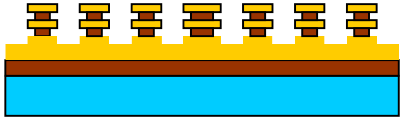
9. SiO_2/Si_3N_4 RIE



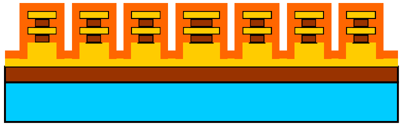
10. Poly wet etching



11. SiO_2 wet etching

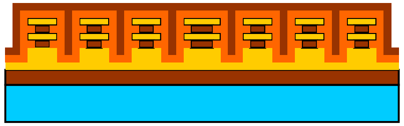


12. Poly deposition

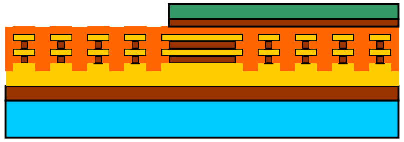


Lateral TEG - process flow (2)

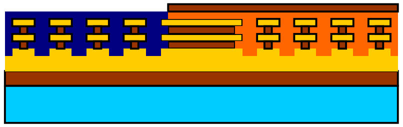
13. SiO_2 deposition



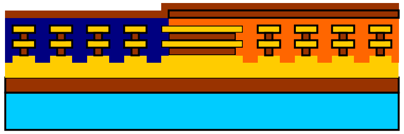
14. SiO_2 wet etching



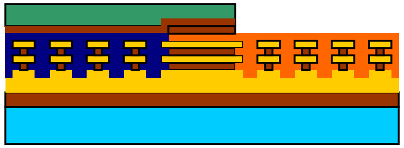
15. P-type doping



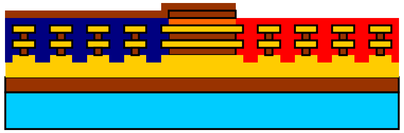
16. SiO_2 deposition



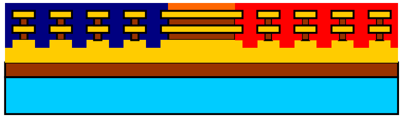
17. SiO_2 wet etching



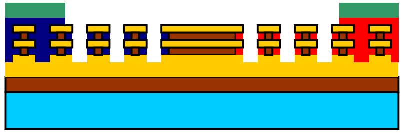
18. N-type doping



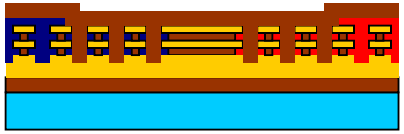
19. SiO_2 wet etching



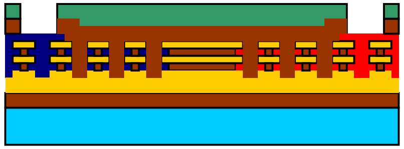
20. Poly RIE



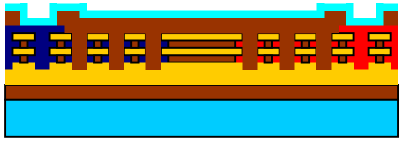
21. SiO_2 deposition



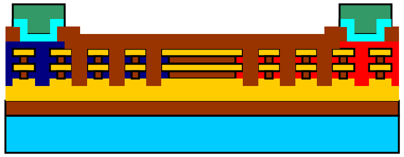
22. SiO_2 wet etching



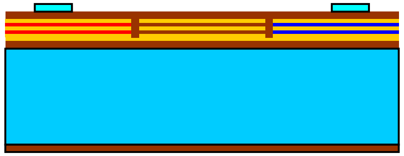
23. Al/Si deposition

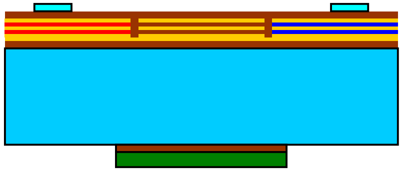


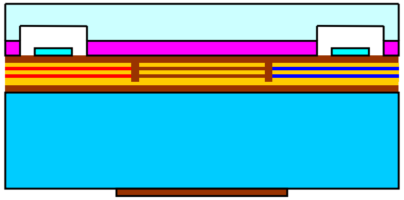
24. Al/Si etching

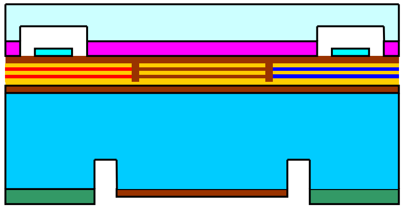


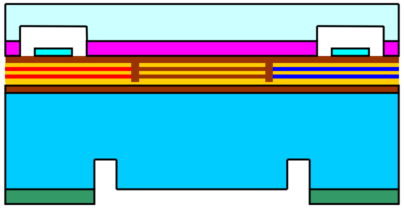
Lateral TEG - process flow (3)

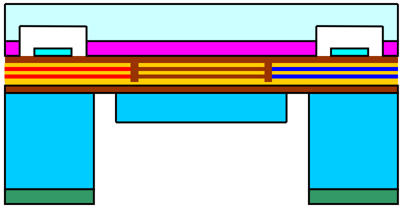

25. Wafer with NWs

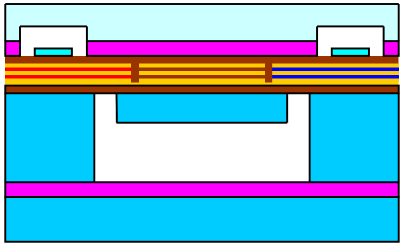

26. SiO_2/Si_3N_4 RIE

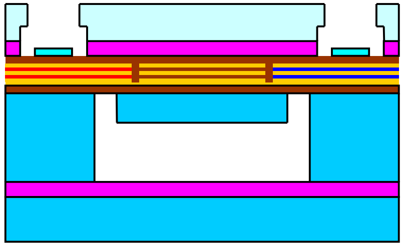

27. Wafer bonding


28. Si DRIE

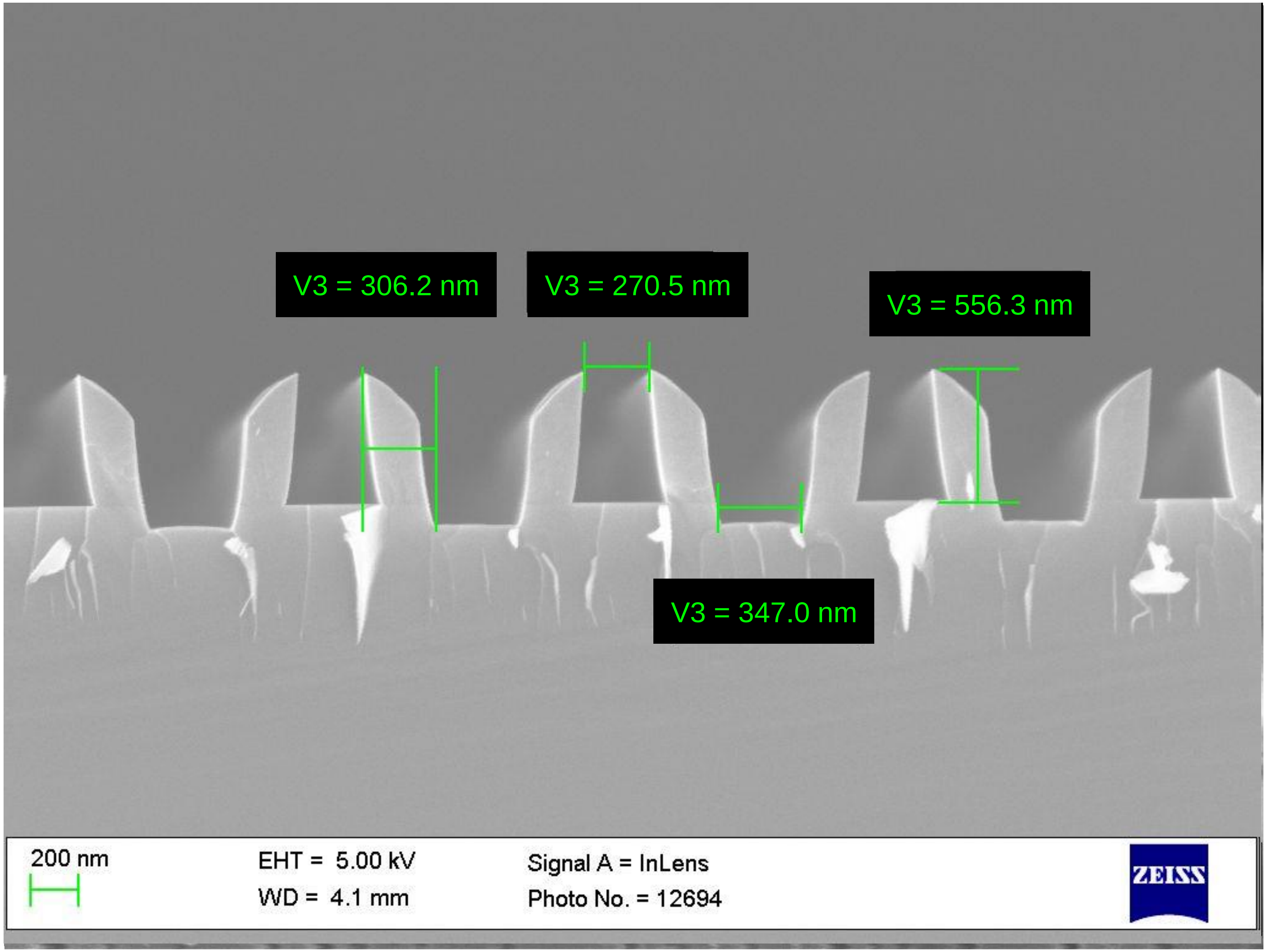

29. SiO_2 etching


30. Si DRIE

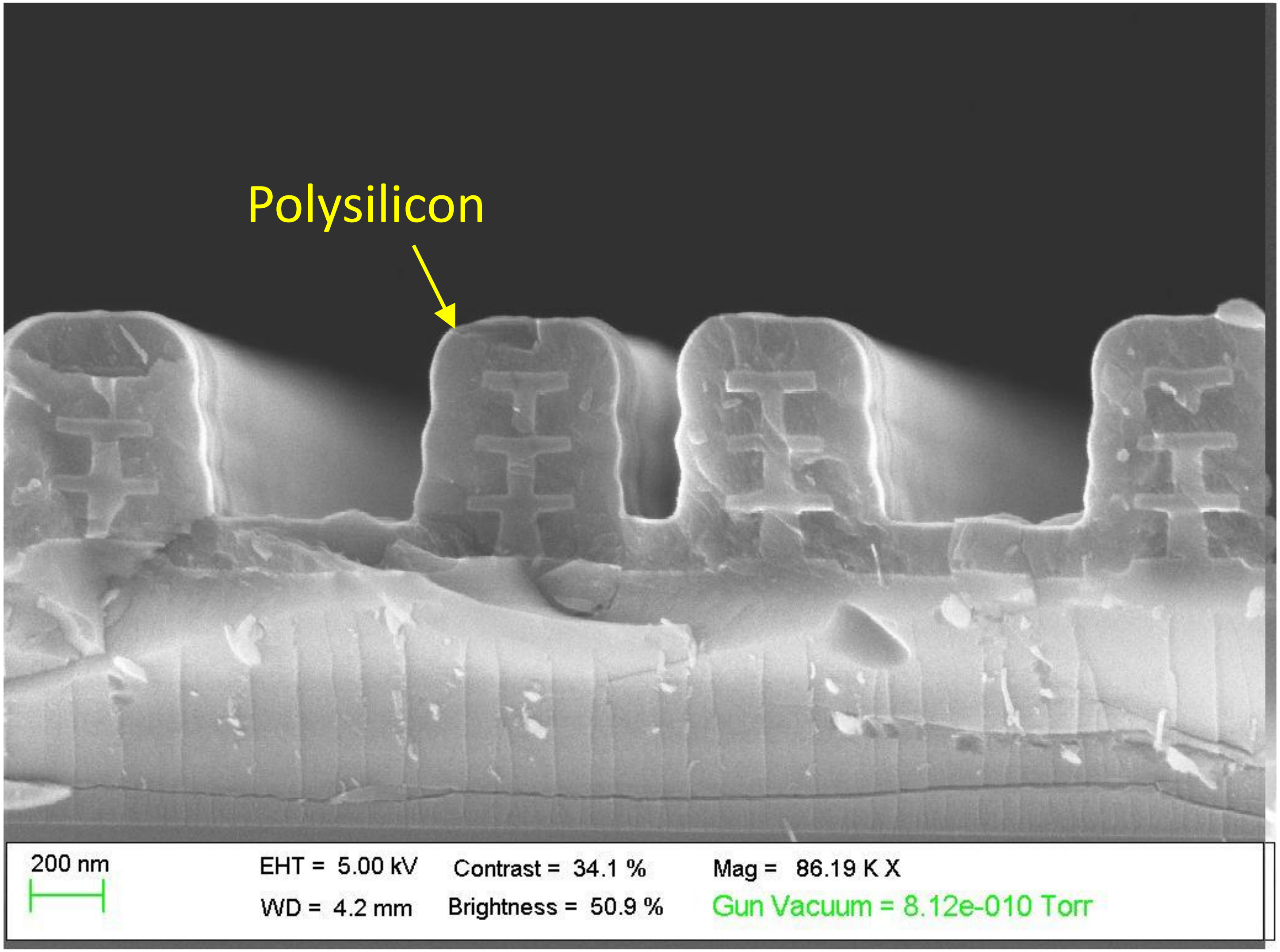

31. Wafer bonding


32. Glass dicing

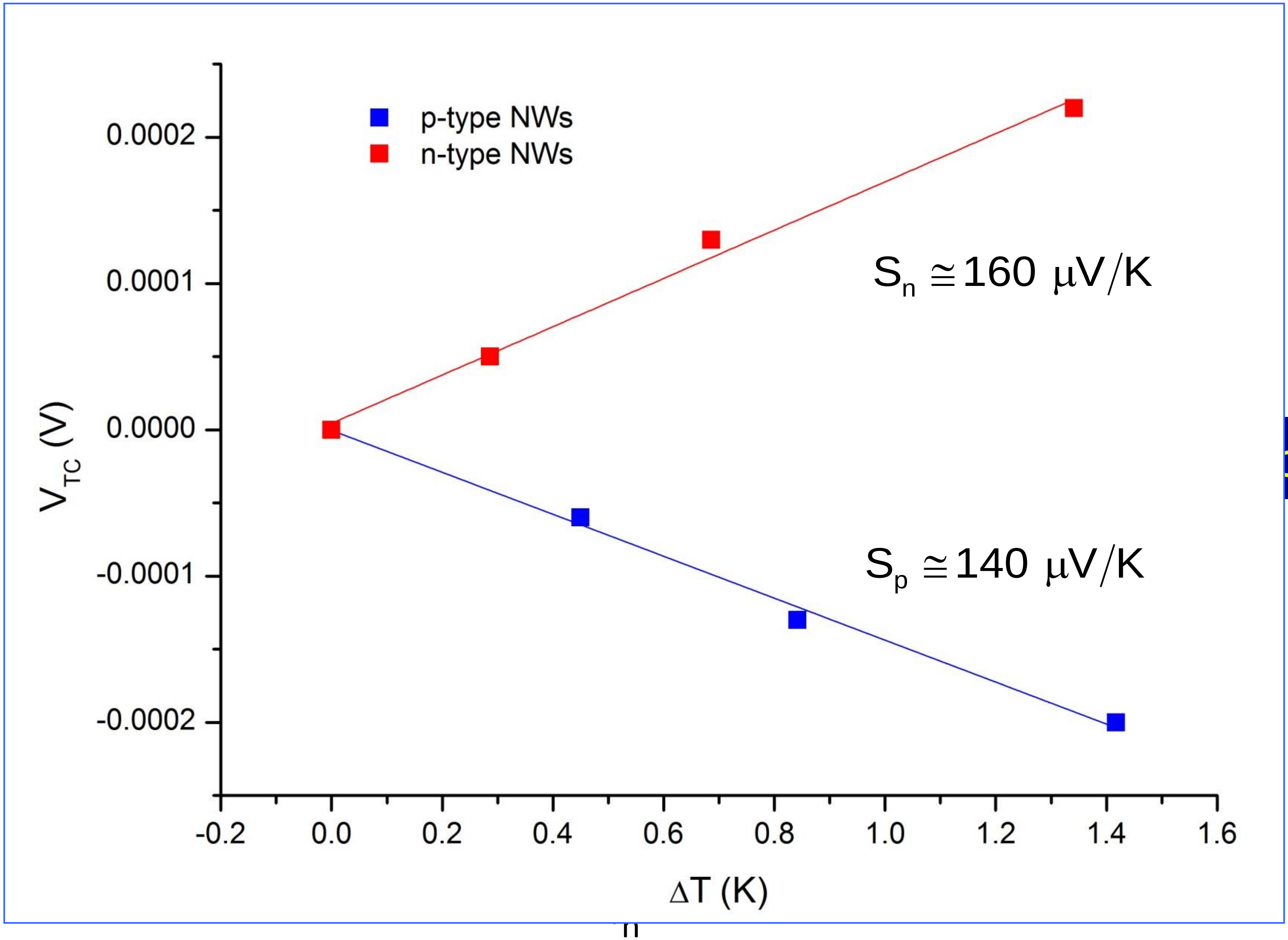
Lateral TEG – Spacers for high-density NWs



Lateral TEG – SiO_2/Si_3N_4 templates for NWs



Lateral TEG – Seebeck measurements on NWs



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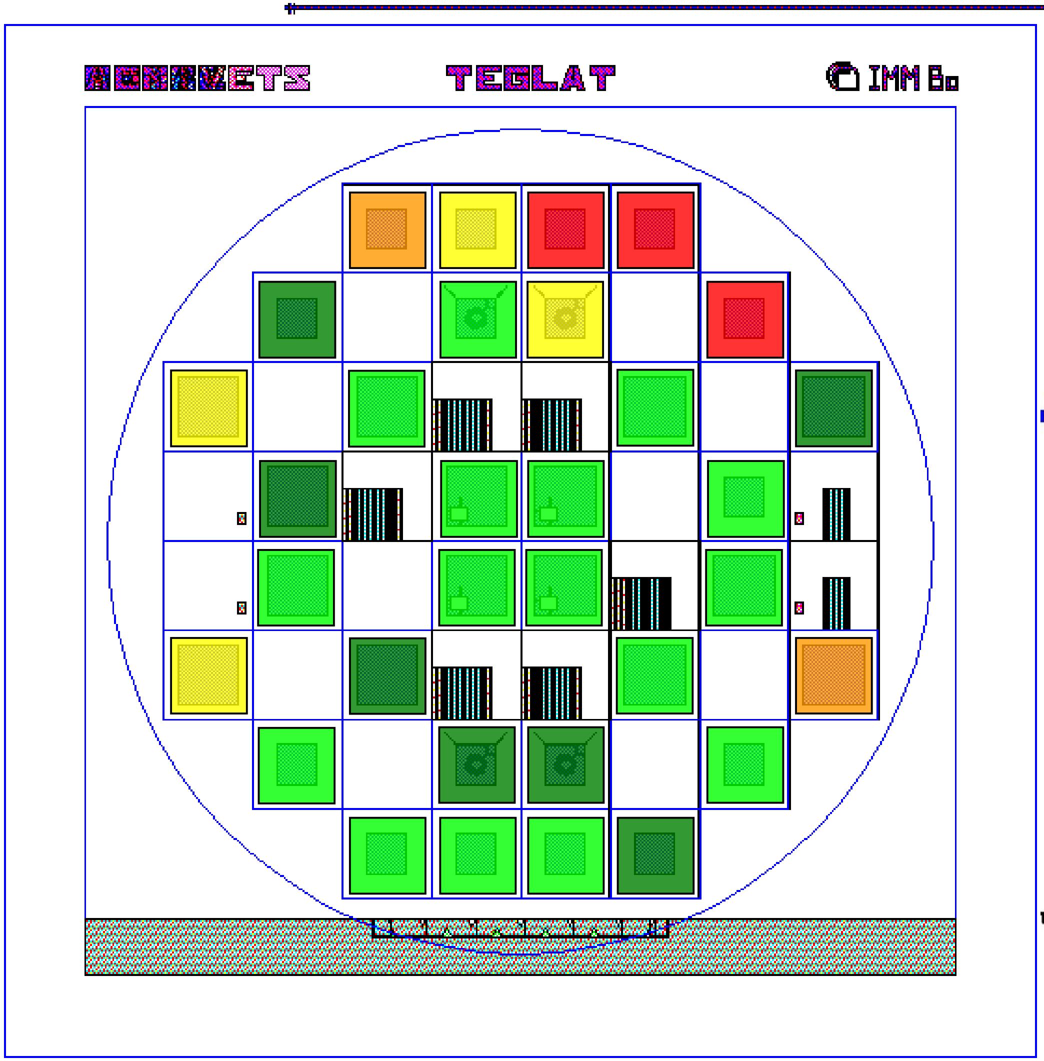
Lateral TEG – Yield test on TEG prototypes



256 Thermocouples in series

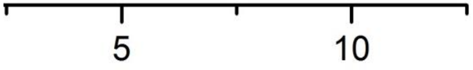
🟩 Fully functional device

🟩 3 working sides

🟨 2 working sides

🟧 1 working side

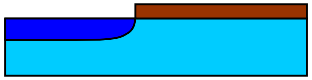
🟥 0 working sides



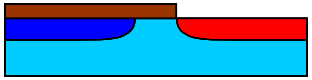
Vertical TEG – Process flow

1. Si substrate

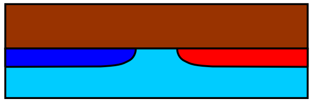
2. P-type doping



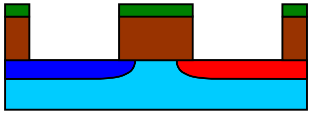
3. N-type doping



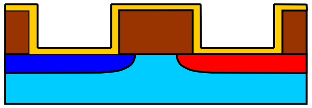
4. Thick SiO_2 deposition



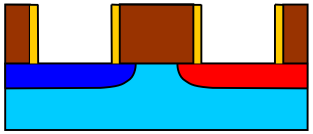
5. SiO_2 RIE



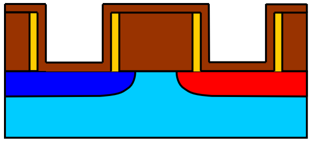
6. Si_3N_4 deposition



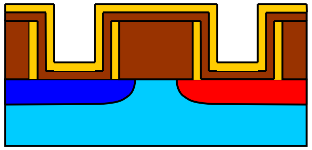
7. Si_3N_4 etchback



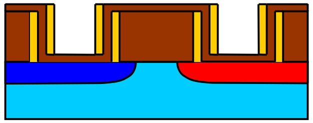
8. SiO_2 deposition



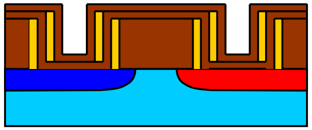
9. Si_3N_4 deposition



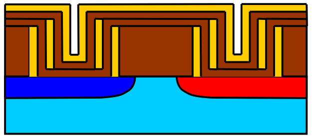
10. Si_3N_4 etchback



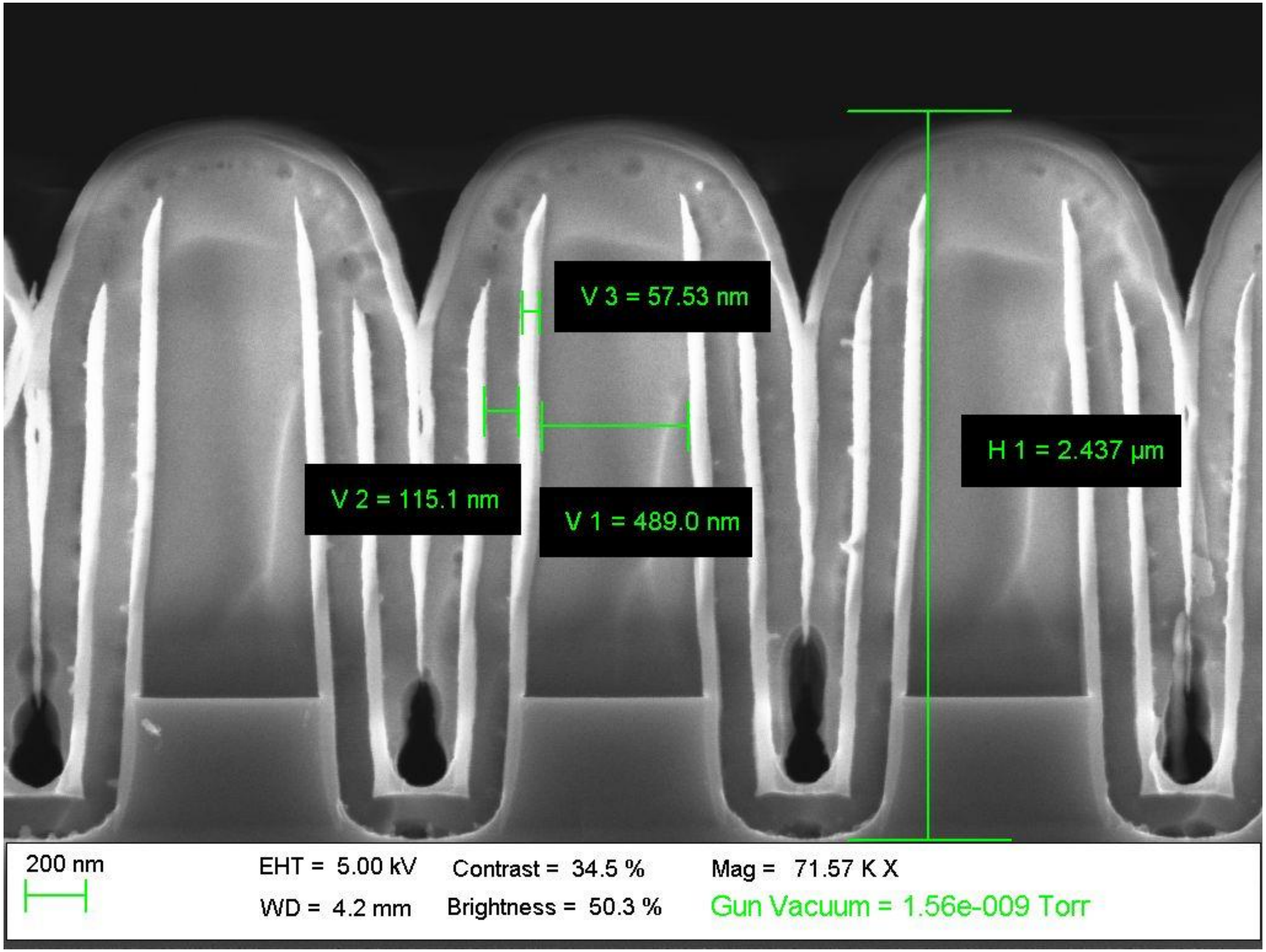
11. SiO_2 deposition



12. Si_3N_4 deposition



Vertical TEG–SiO_2/Si_3N_4 templates for high-density NWs



Summary

- Lateral NW arrays with linear density of 1.0×10^4/mm have been obtained.
- On the high-density lateral NWs, electrical resistivity values around 2.0 mΩ cm with n-type doping and 4.0 mΩ cm with p-type doping have been achieved.
- The measured Seebeck coefficient was around 150 µV/K for both doping types.
- An overall functionality above 80% has been obtained on lateral TEG prototypes in yield tests.
- The fabrication of vertical TEGs is ongoing. Early results on the fabrication of high-density templates for vertical NWS have been obtained.

Conclusions

- Both top-down and bottom-up approaches to TEGs could achieve their target as of nominally available power density.
- Next targets of WP2 will be
  - assembling and wiring the chips
  - packaging
  - testing (benchtop, simulated, and actual scenario)

The Thermoelectric Team

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sinergy-project.eu
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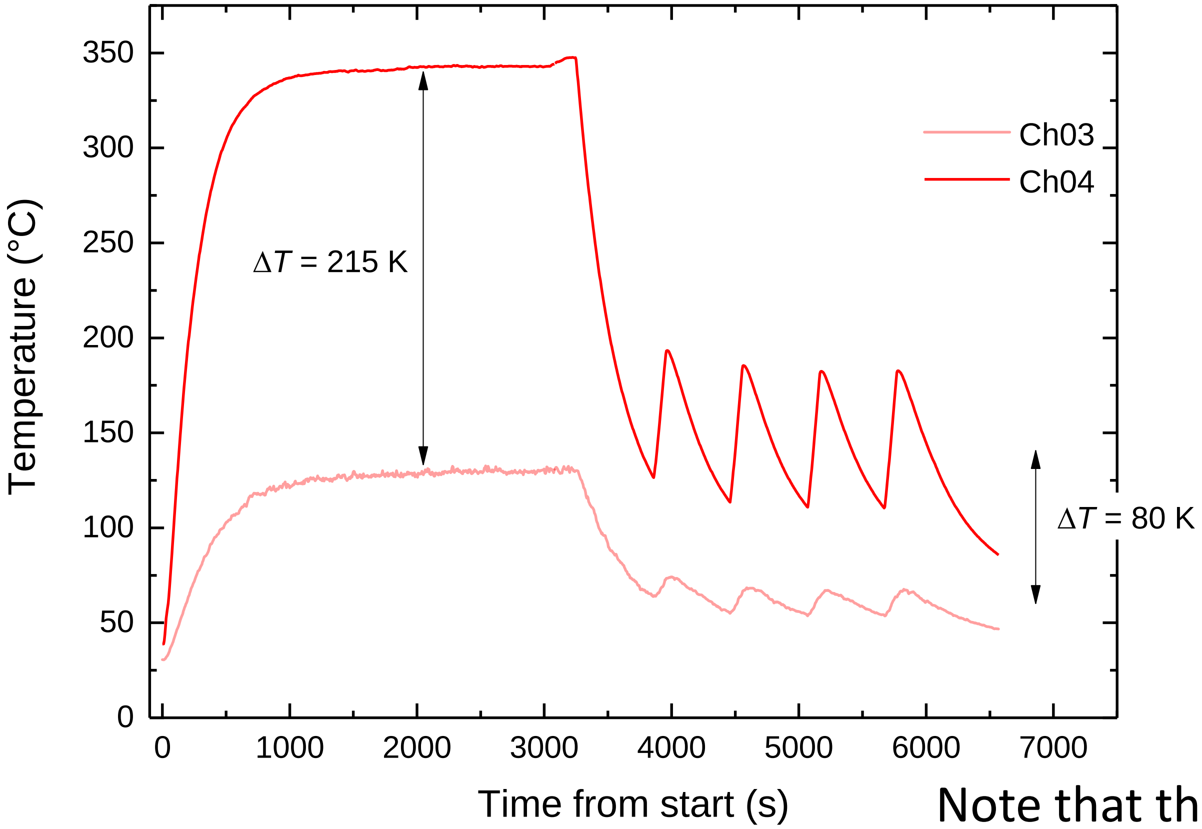
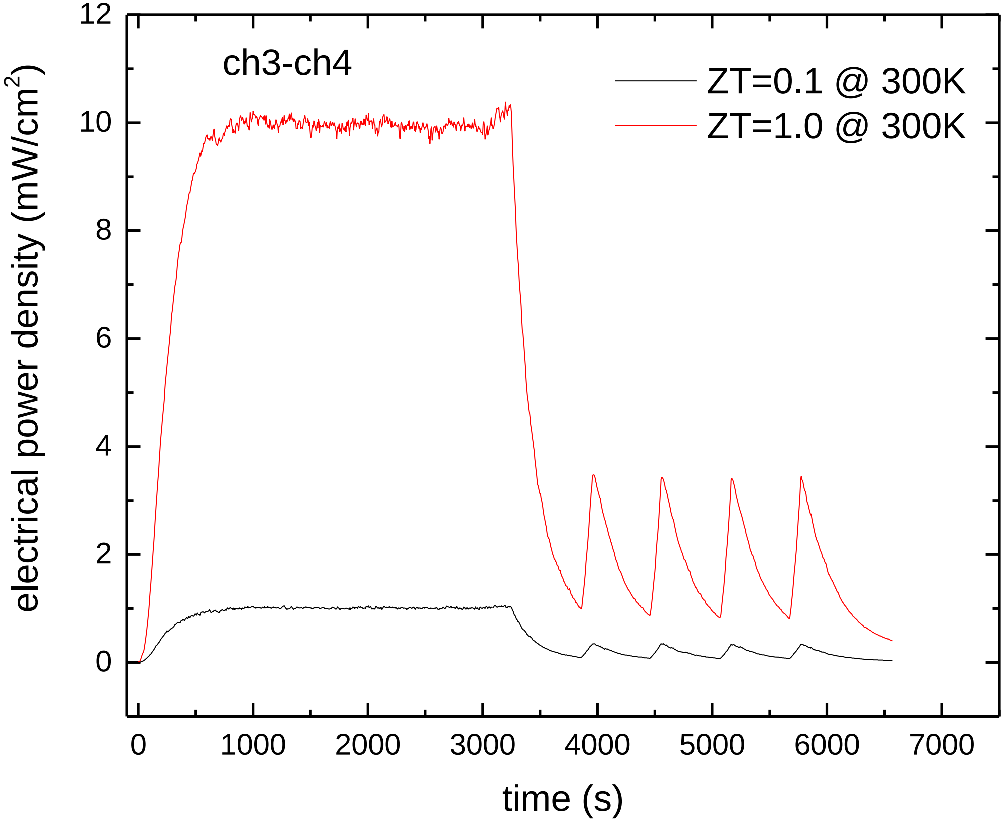
Application scenario:



Note that the harvester cold side will have to dissipate heat in steady air

Application scenario: Industrial Fryers



Minimal needed power estimated considering that the average input electric power required by RF module to read temp + transmit data at 3V is
3.5 to 4μW for transmission each 10 s
1.3 to 1.5μW for transmission each 60 s

Average power during pulse transmission (6 ms) is 2.7mW.

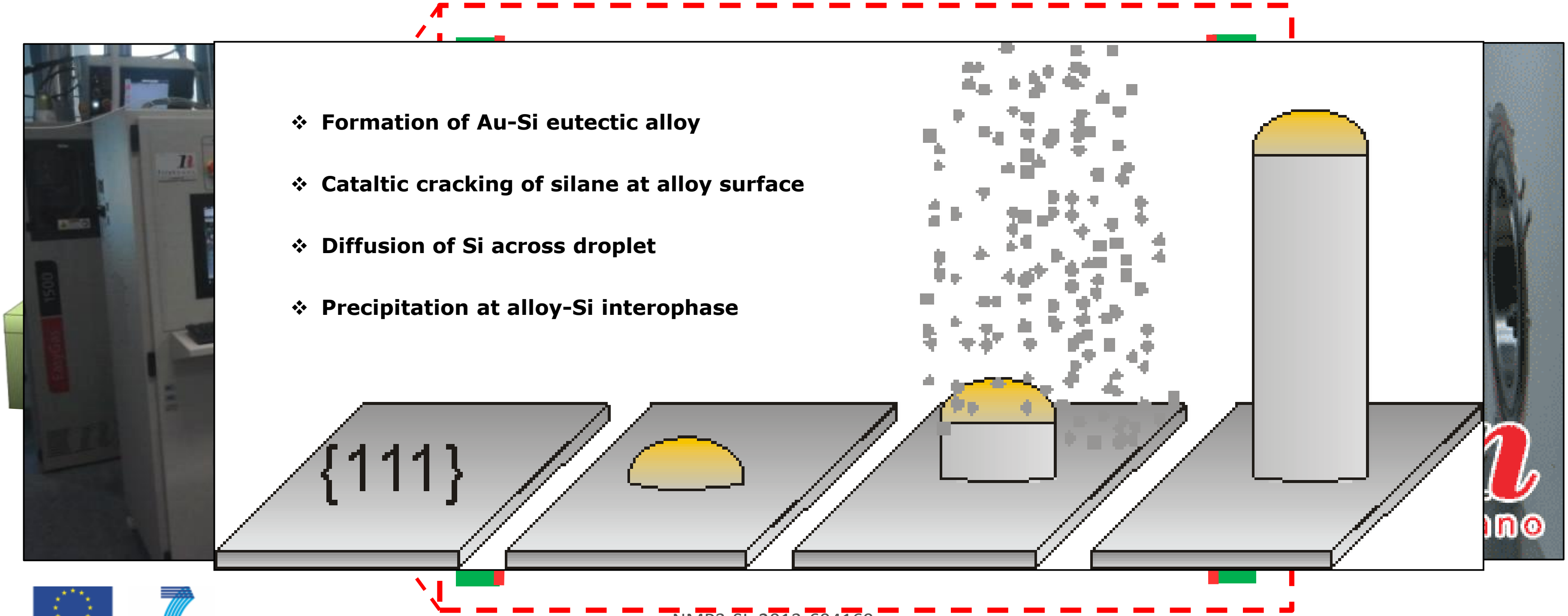
Instantaneous peak power can be up to 75mW. A large capacitor (22μF) will be placed after the power management unit.

CVD-VLS growth of silicon nanowires

1 – Devices are dipped in **HF** in order to remove thermal oxide formed druing calcination

2 – Devices are loaded into **CVD**

3 – There devices are brought to **reaction conditions and exposed to silane.** Silicon nanowires are grown by VLS synthesis

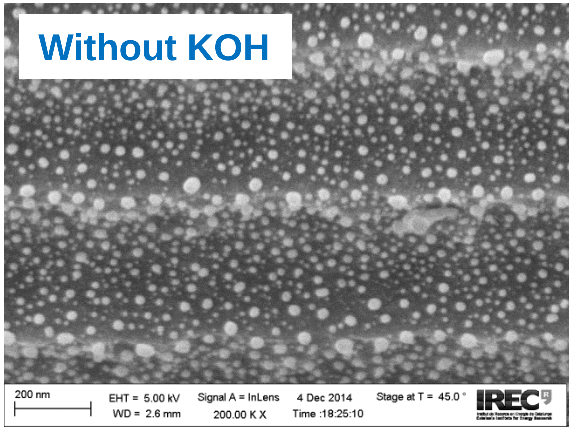


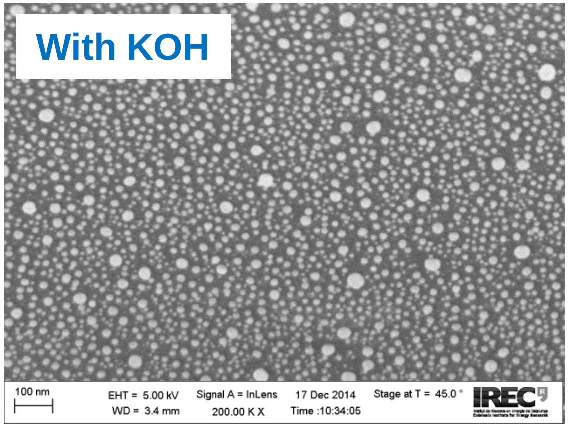
- **Formation of Au-Si eutectic alloy**
- **Cataltic cracking of silane at alloy surface**
- **Diffusion of Si across droplet**
- **Precipitation at alloy-Si interophase**

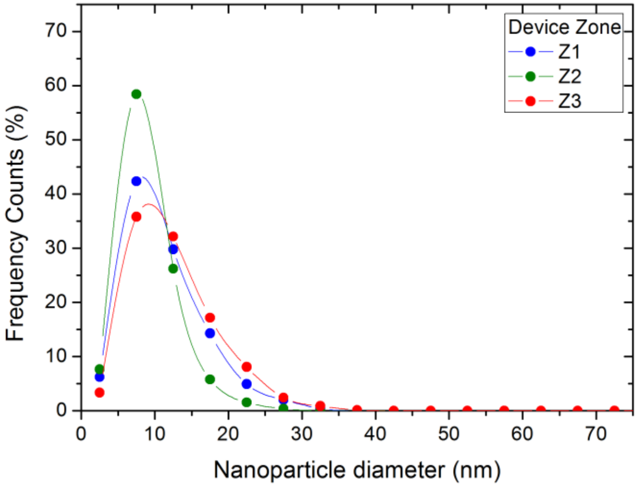
Gold deposition – Galvanic displacement

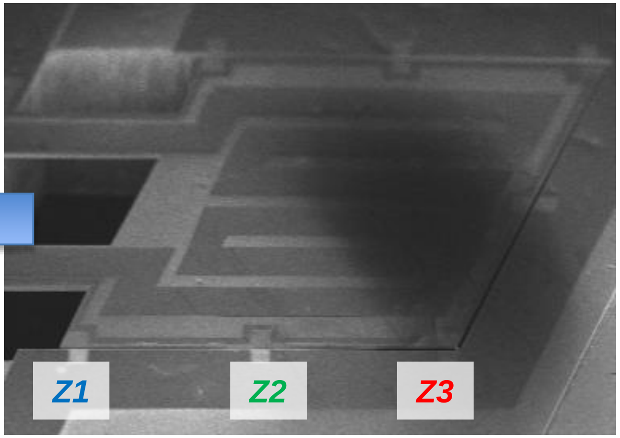
Looking for a higher control of the galvanic displacement

1. ***Analysis of the gold homogeneity in the trenches***
2. *Influence of the trench width and the structure itself on the gold deposit*









Gold deposition – Galvanic displacement

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1. ***Analysis of the gold homogeneity in the trenches***
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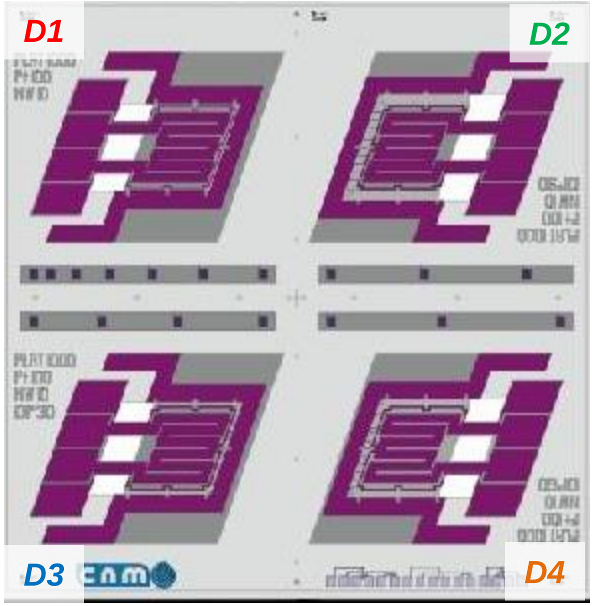

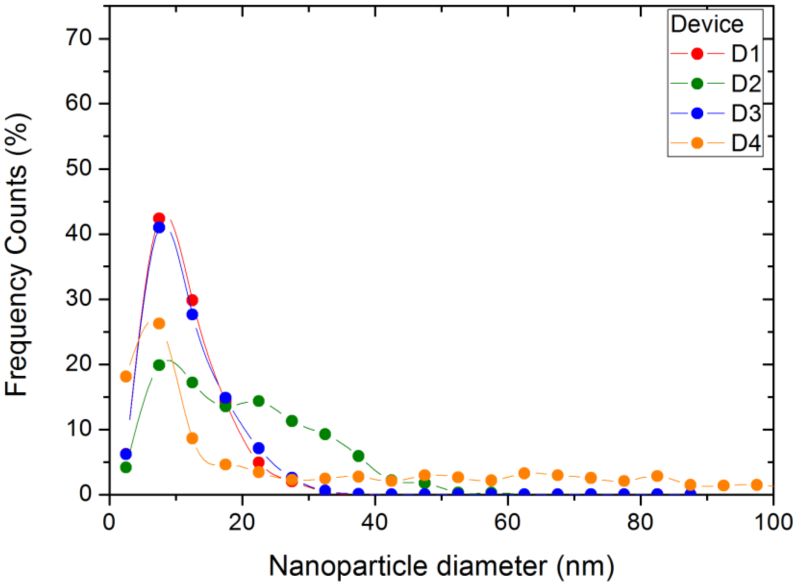

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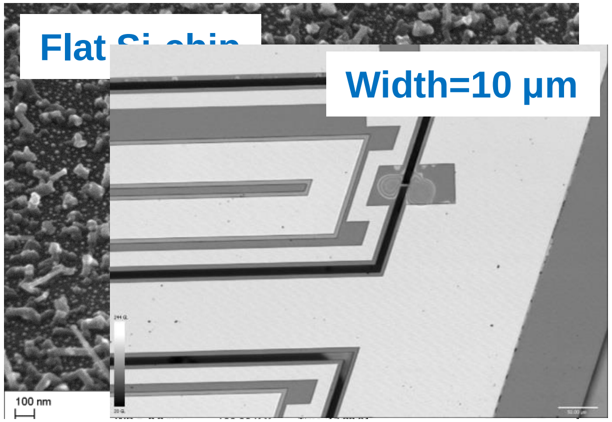

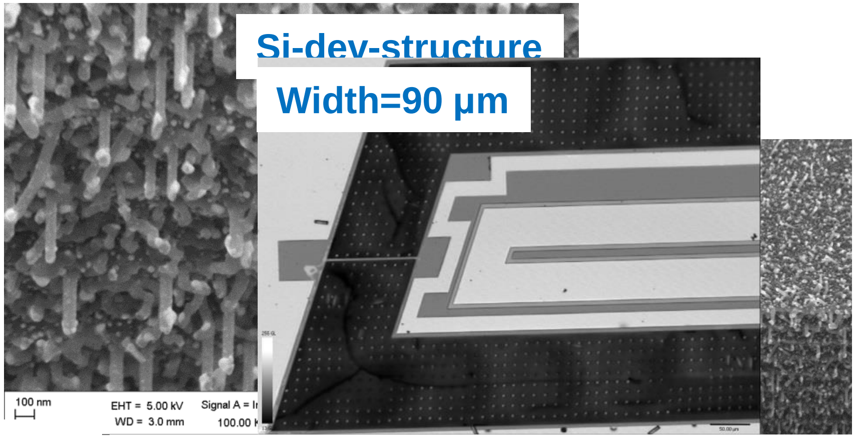

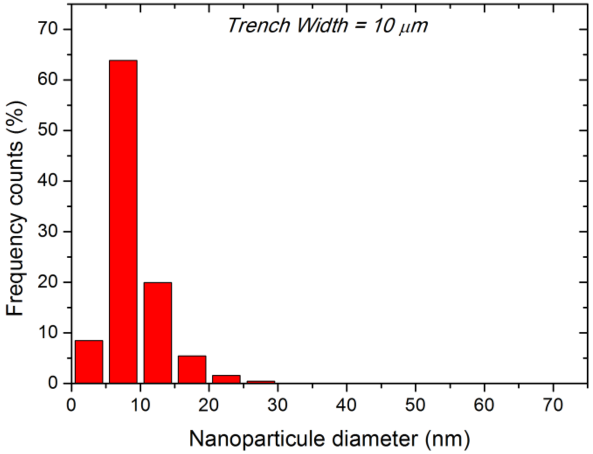

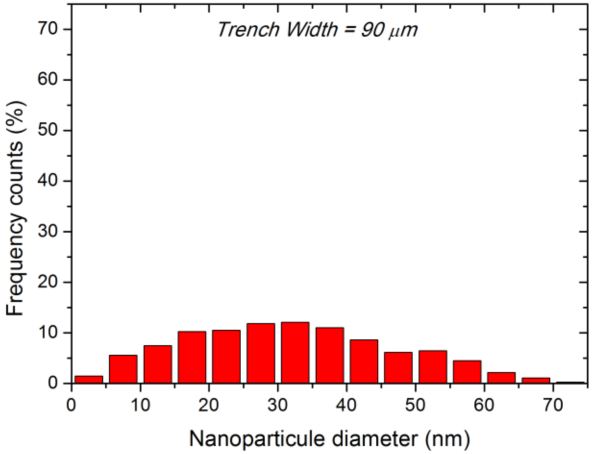

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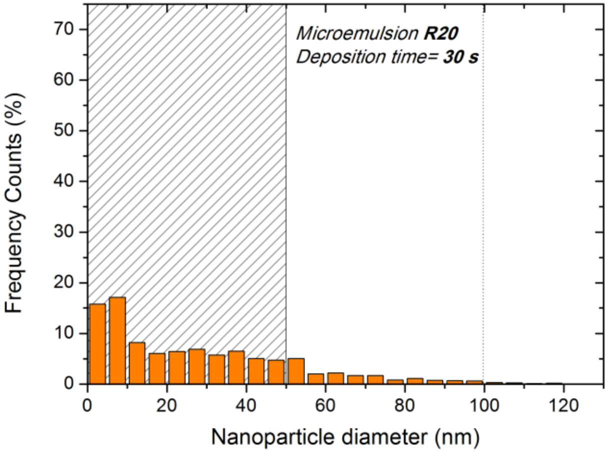
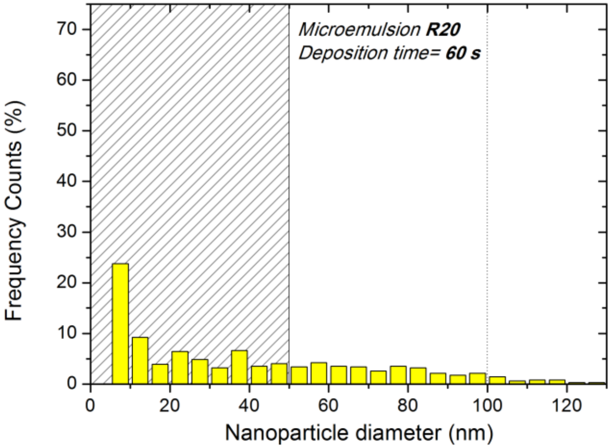
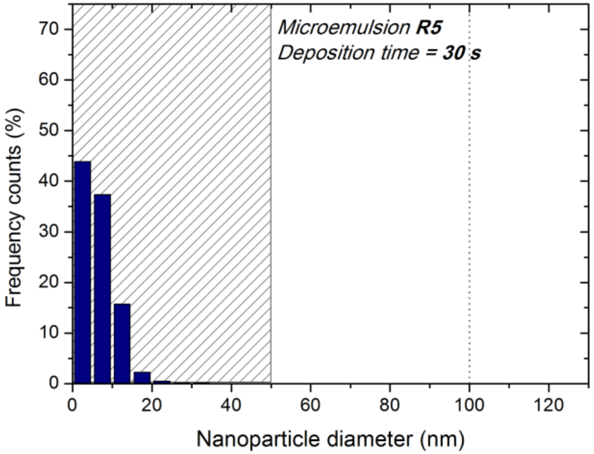
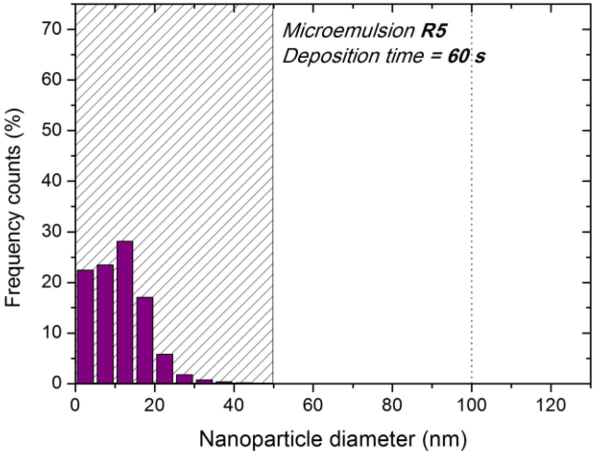
R20





R5

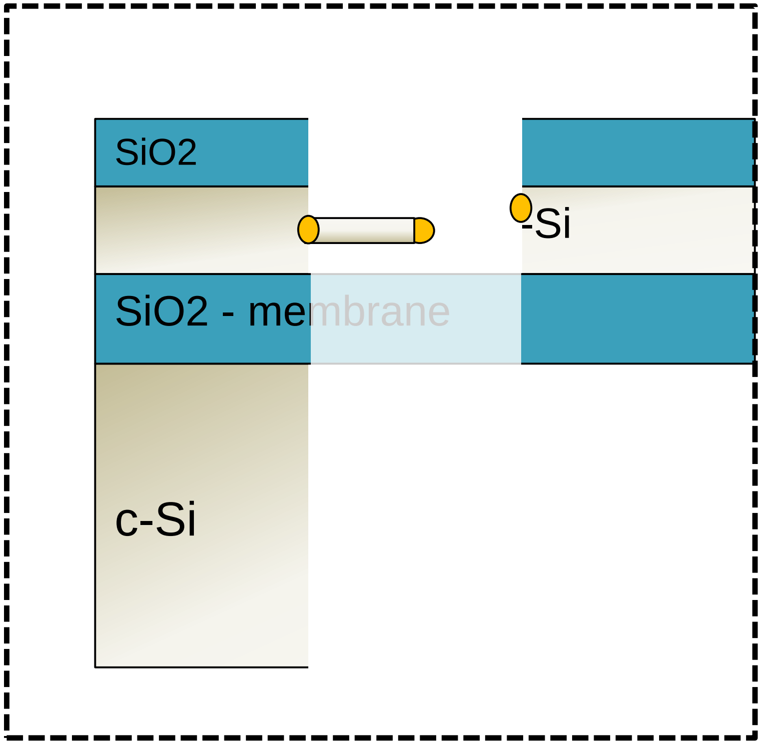


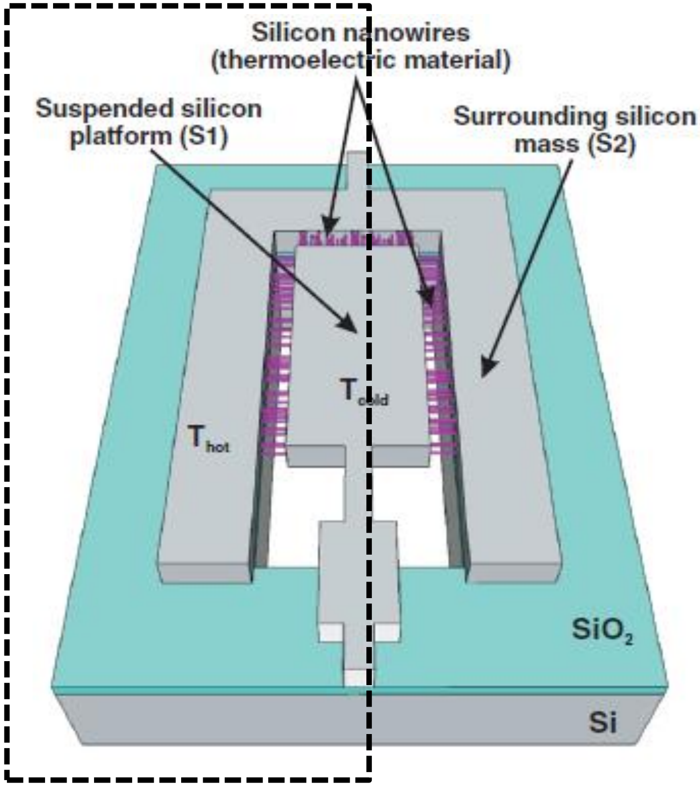


General Scheme

Main steps in the fabrication process

1. *Gold deposition – Galvanic displacement*
2. ***SiNW growth – CVD process***
3. *μTEG basic thermoelectric characterization*

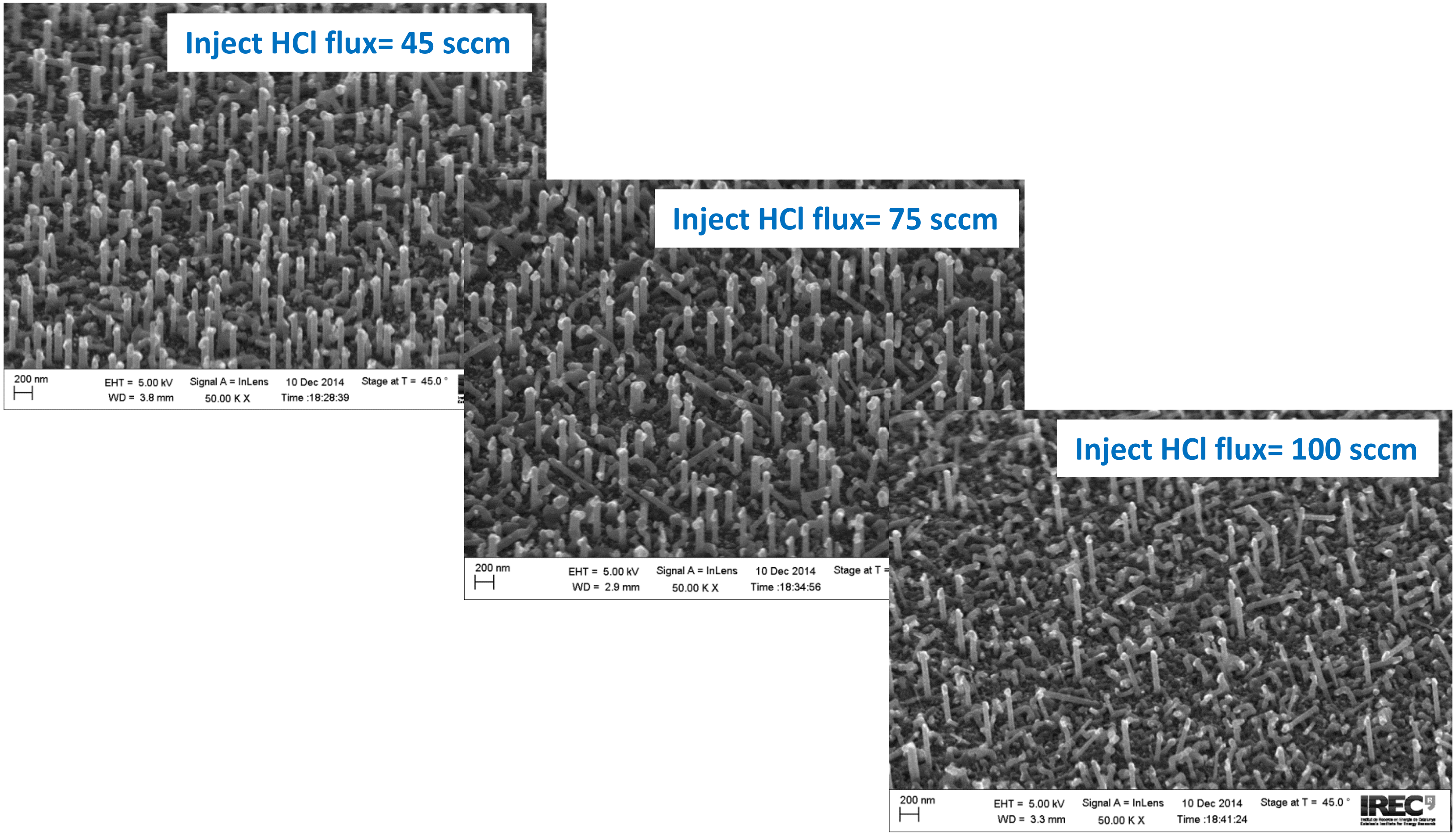




SiNW growth – CVD process

Control of the SiNW array characteristics

1. ***Influence of the HCl pre-inject step on array density***
2. *Preliminary p-doped SiNW electrical measurements*



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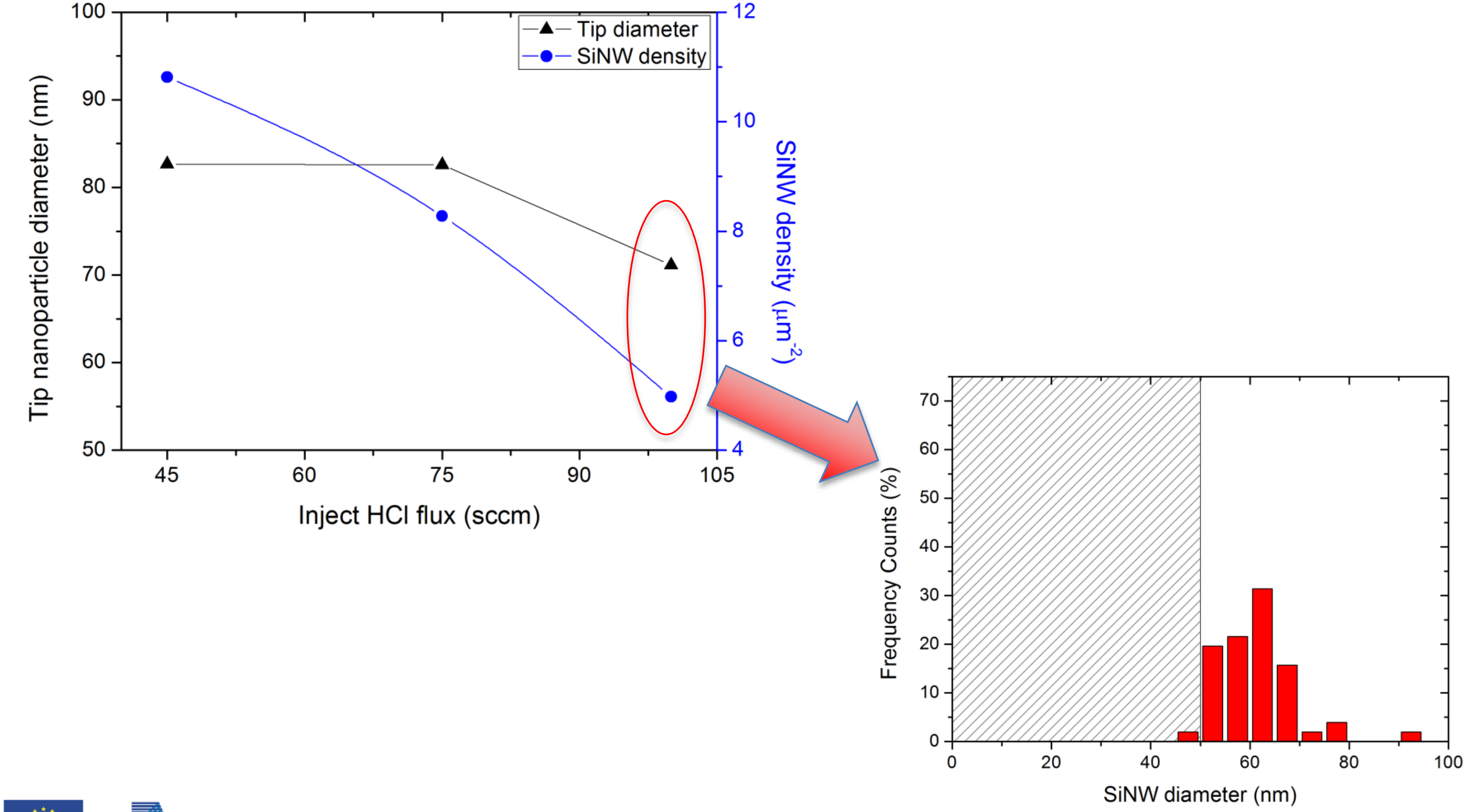

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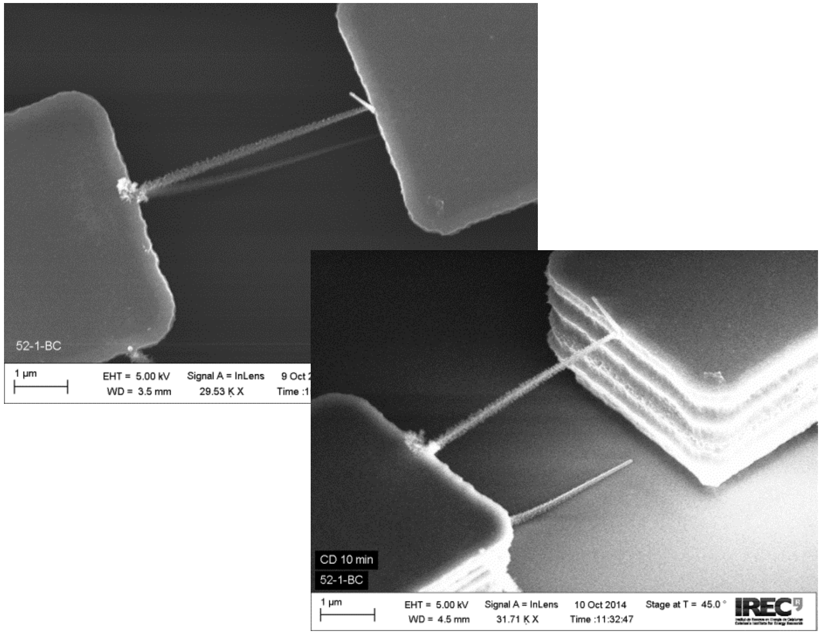
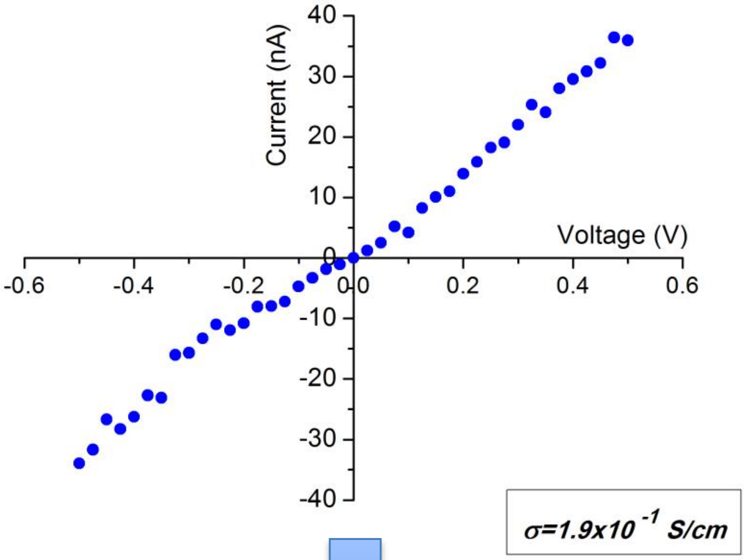
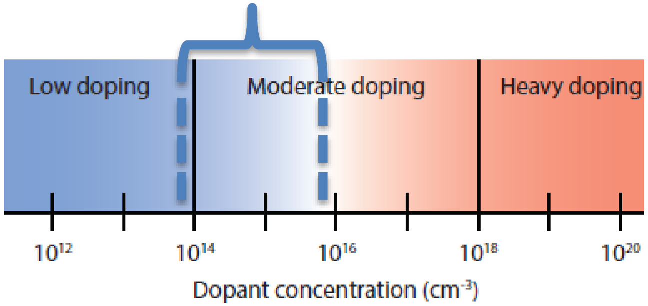




σ=1.9x10^{-1} S/cm

SiNW dopant concentration (in-situ doping)

1×10^{14} - 1×10^{16} cm^{-3}



The range of doping levels used in c-Si.

SiNW growth – CVD process

Control of the SiNW array characteristics

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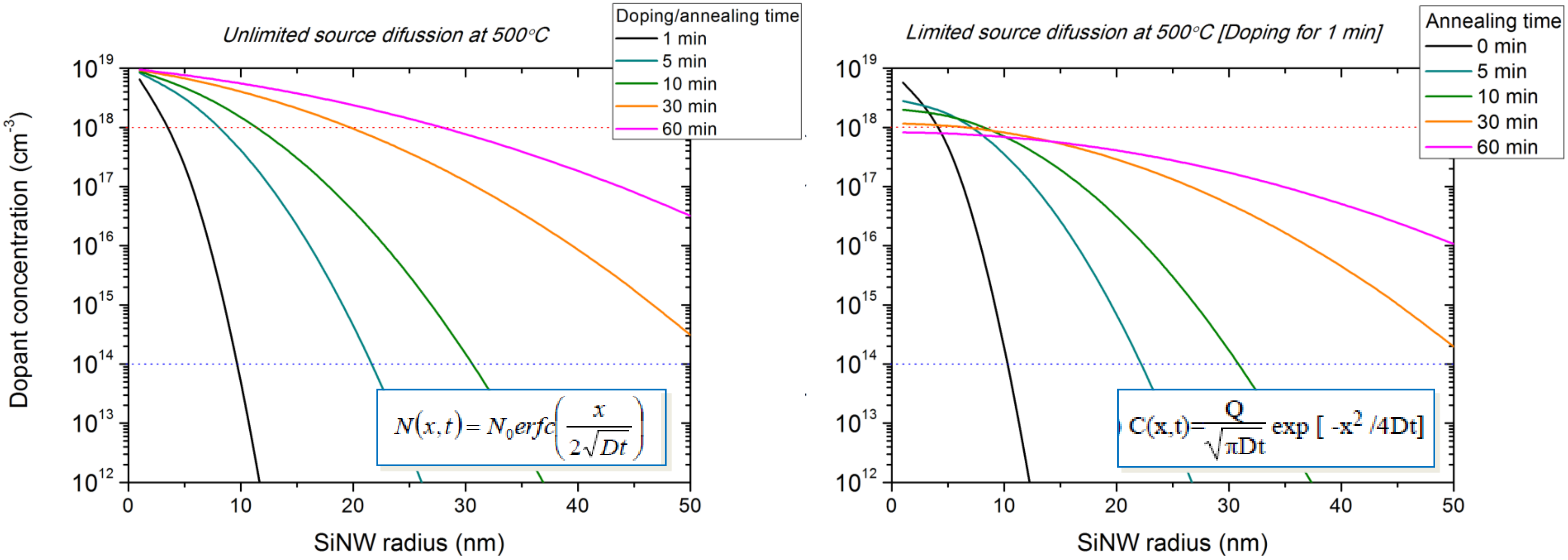
W. Chen et al. - J. Appl. Phys. 111, 094909 (2012)

B difussion coefficient in SiNW at 500ºC - D=4.22 ×10^{-16} cm^2/s

*SiNW dopant concentration (**ex-situ doping**)*



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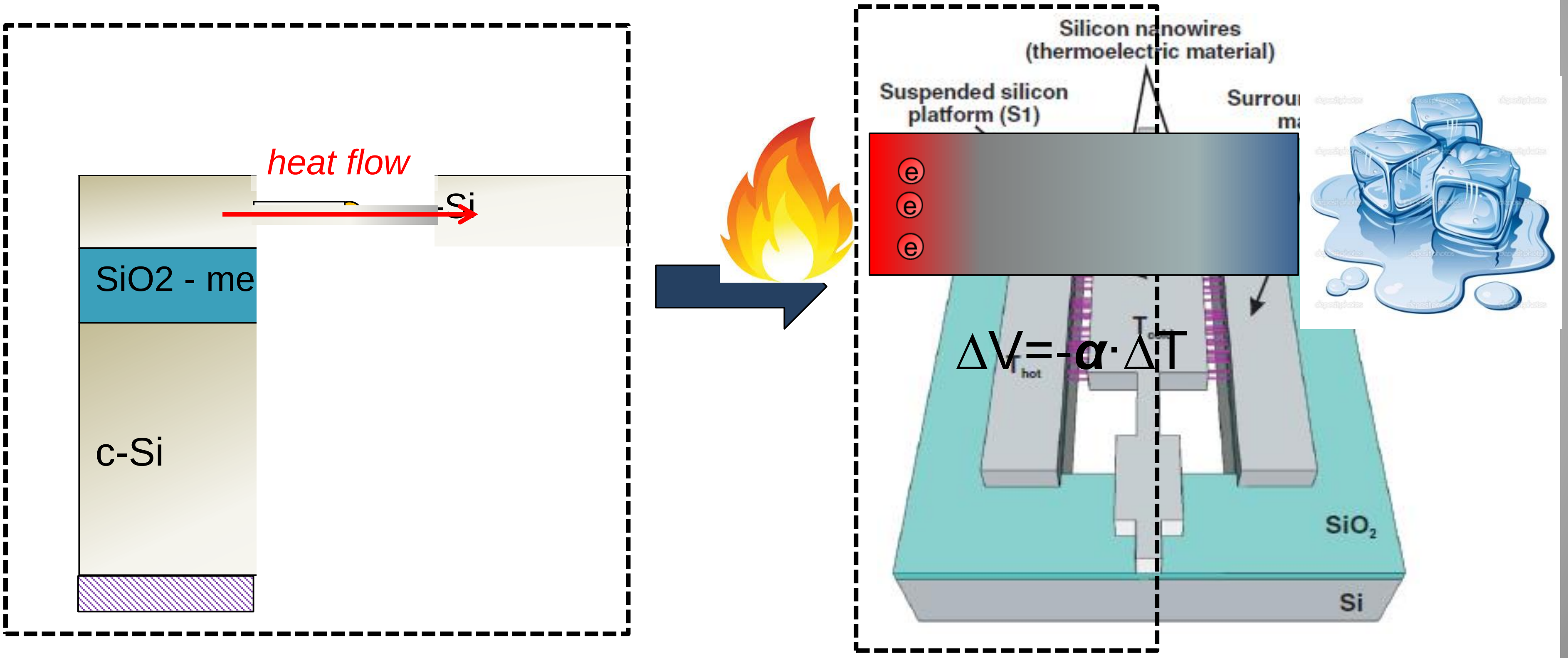
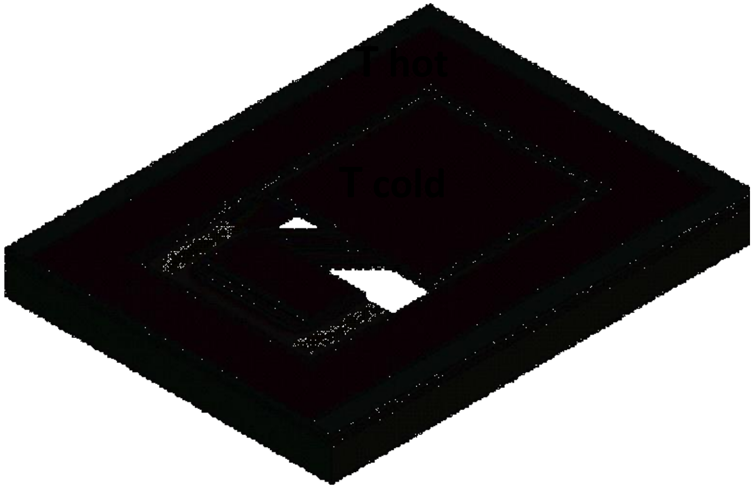


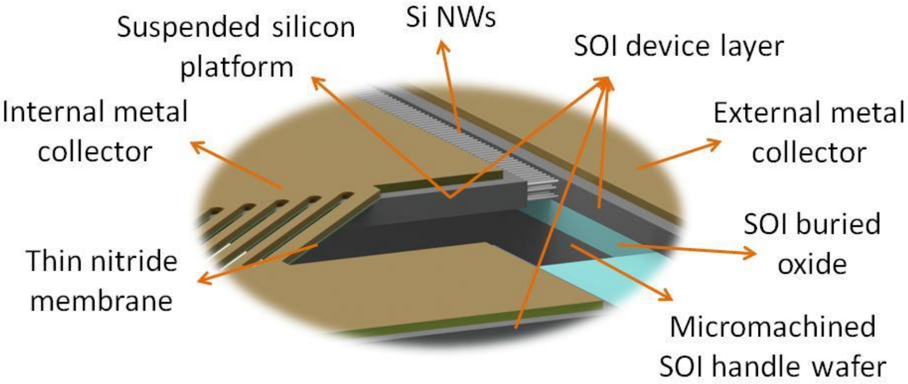
Conclusions

New results in the fabrication process at IREC

- ***Gold deposition***
  - *The Au particle size distribution present high uniformity (top to bottom/along the trenches) after KOH etching and SiO_2 membrane elimination.*
  - *Gold microemulsion and deposition time have to be optimized for each device structure. Nanoparticle diameter lower than critical diameter for SiNW growth (d_c=50 nm) are preferable.*
- ***SiNW growth***
  - *Combined with small Au nanoparticles ($d<d_c$), the HCl pre-inject flux allows to control the SiNW density.*
  - *Preliminary electrical measurements confirm a low SiNW doping level. Ex-situ doping could lead to higher and more uniform doping levels.*
- ***µTEG basic characterization***
  - *Low doping level would be responsible for low power values. Simulations confirm that a SiNW conductivity increase would lead to noticeably improve the P_{MAX}.*
  - *The control of the SiNW array density would have an important impact on the performance of the device. Different SiNW properties and/or device structure characteristics will require an array density optimization.*

Bottom-up strategy – Si platforms





Suspended silicon platform

Si NWs

SOI device layer

Internal metal collector

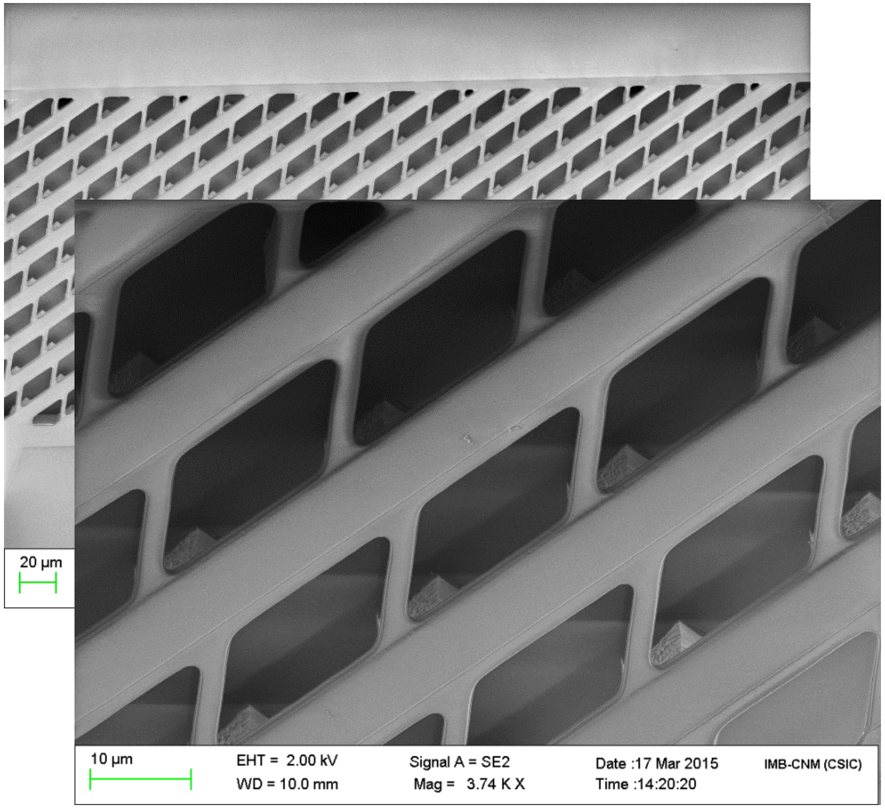
External metal collector

SOI buried oxide

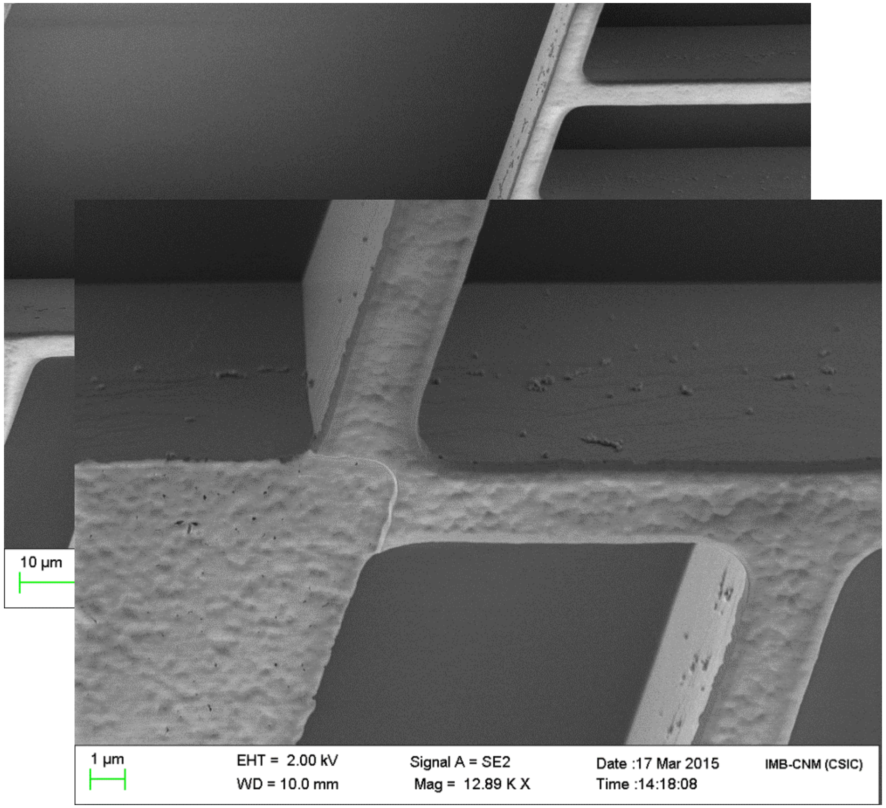
Thin nitride membrane

Micromachined SOI handle wafer

Si platforms



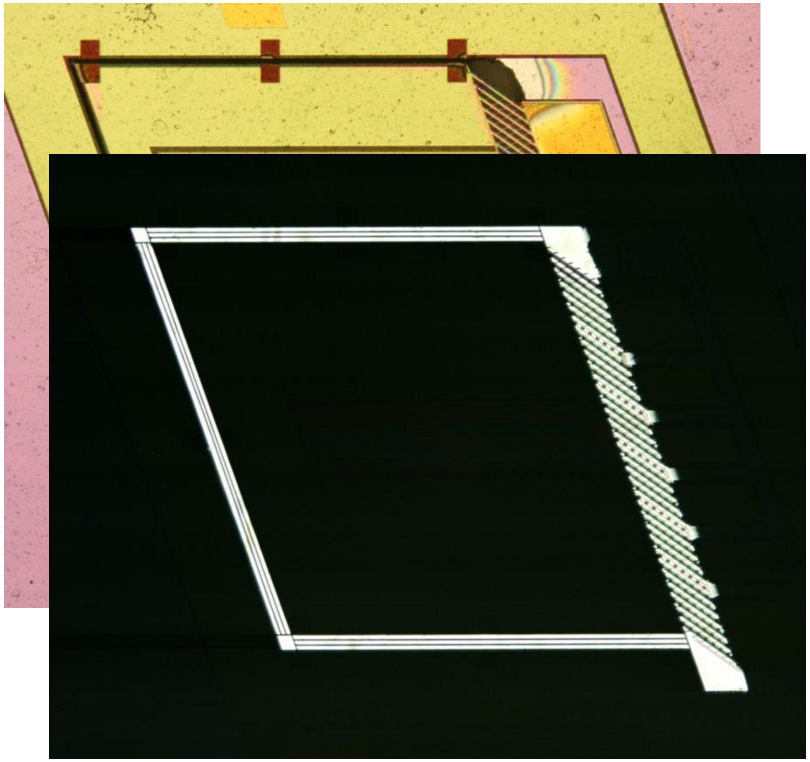
Sacrificial Si

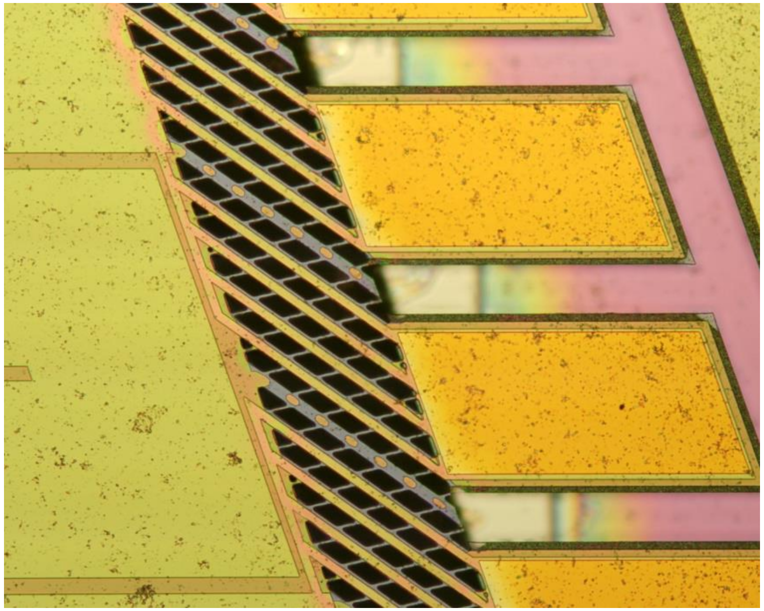


Durable Si

Bottom-up strategy – Si platforms

- Buried oxide removed with HF vapors after DRIE on the back side.

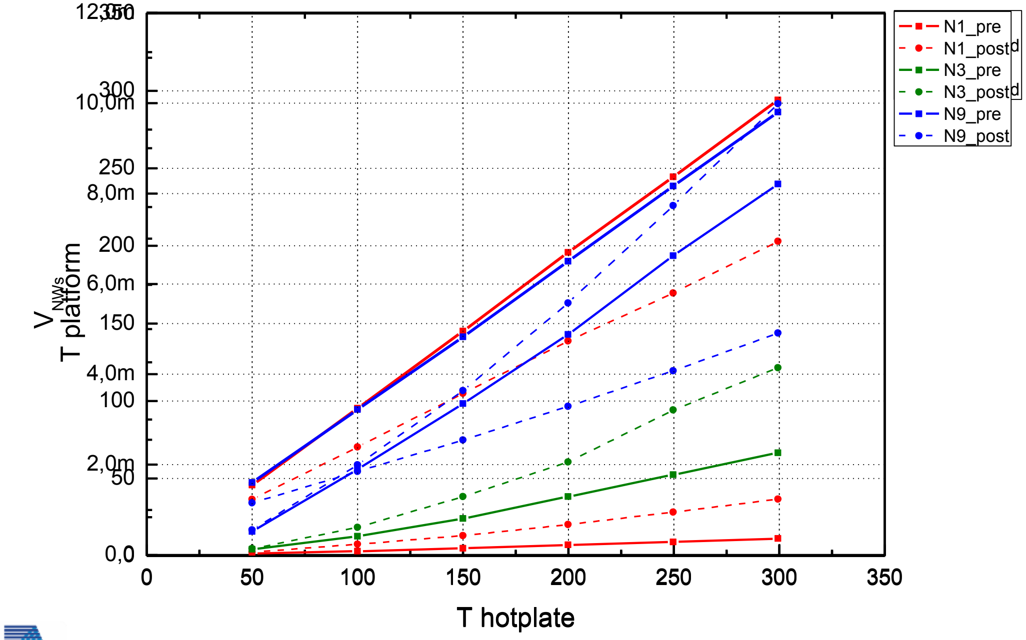


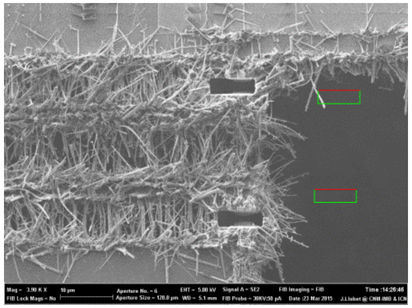


- Resist removed with plasma etch

Bottom-up strategy – Measurements

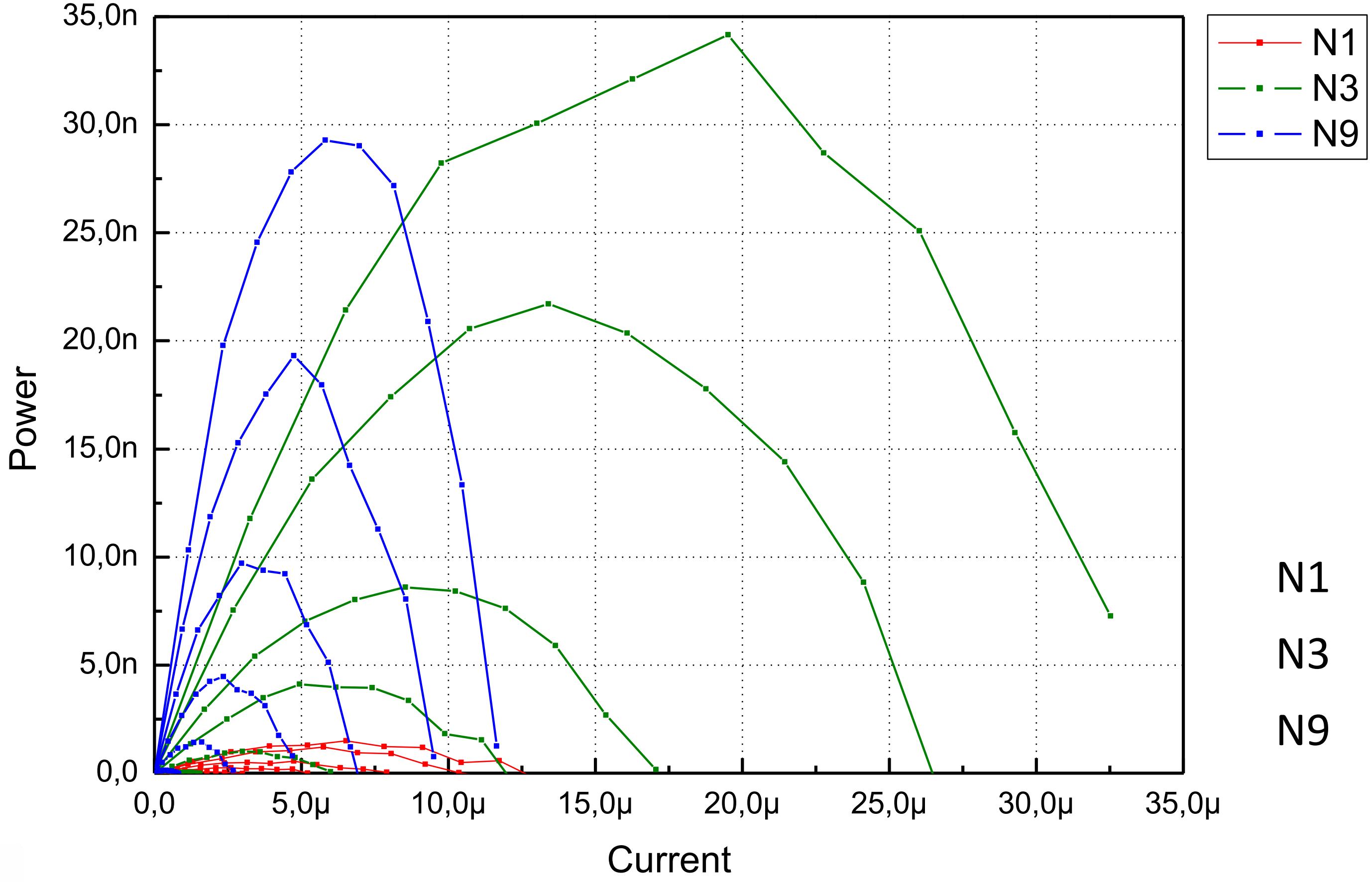
- Thermovoltage and thermopower obtained in several harvesting conditions were determined for devices with different number of NWs arrays.
- Forced convection was used to improve ΔT.
- Silicon temporary supports were removed by FIB.





Bottom-up strategy – Measurements

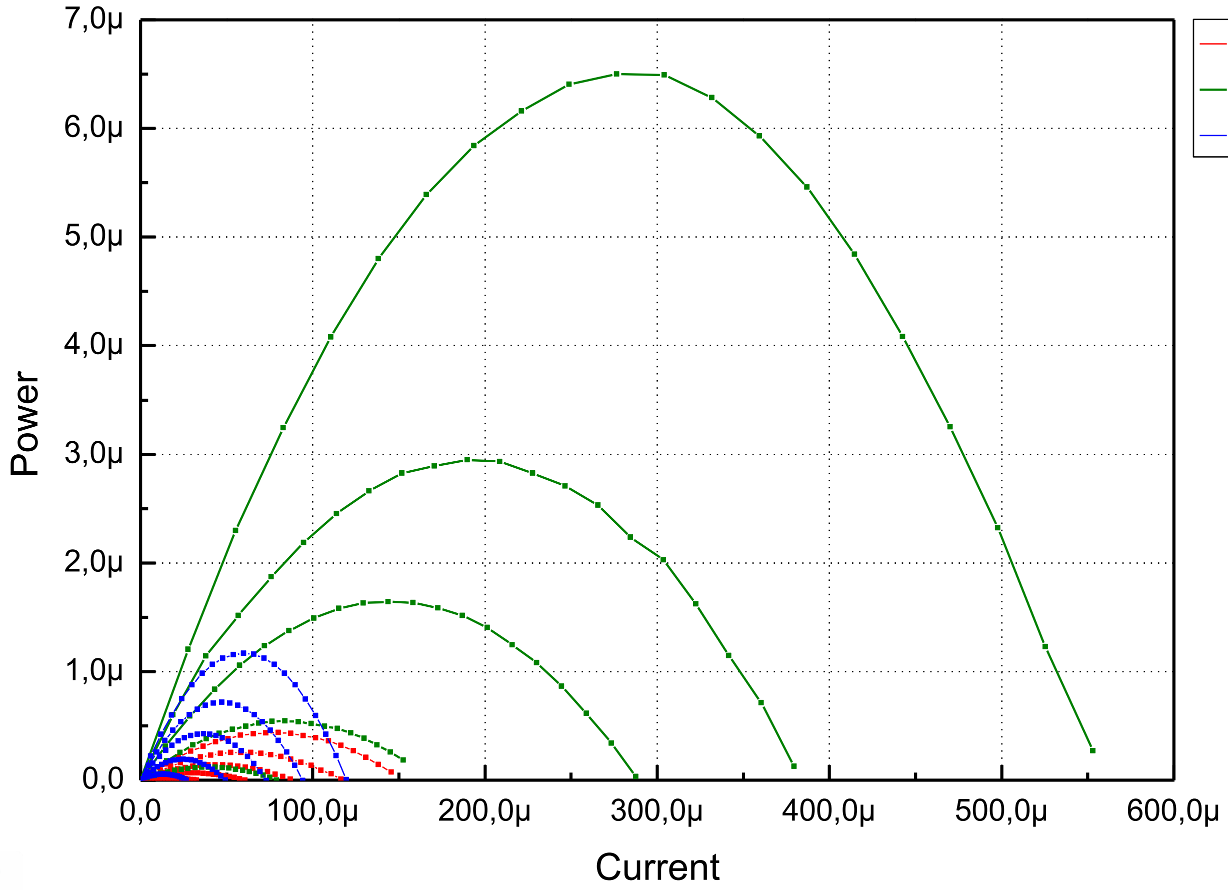
- Power curves. Harvesting mode with T of the hotplate up to 250 ºC.



	R_{NW} (Ω)
N1	46
N3	93
N9	700

Bottom-up strategy – Measurements

- Power curves. Test mode with ∆T up to 100 ºC.

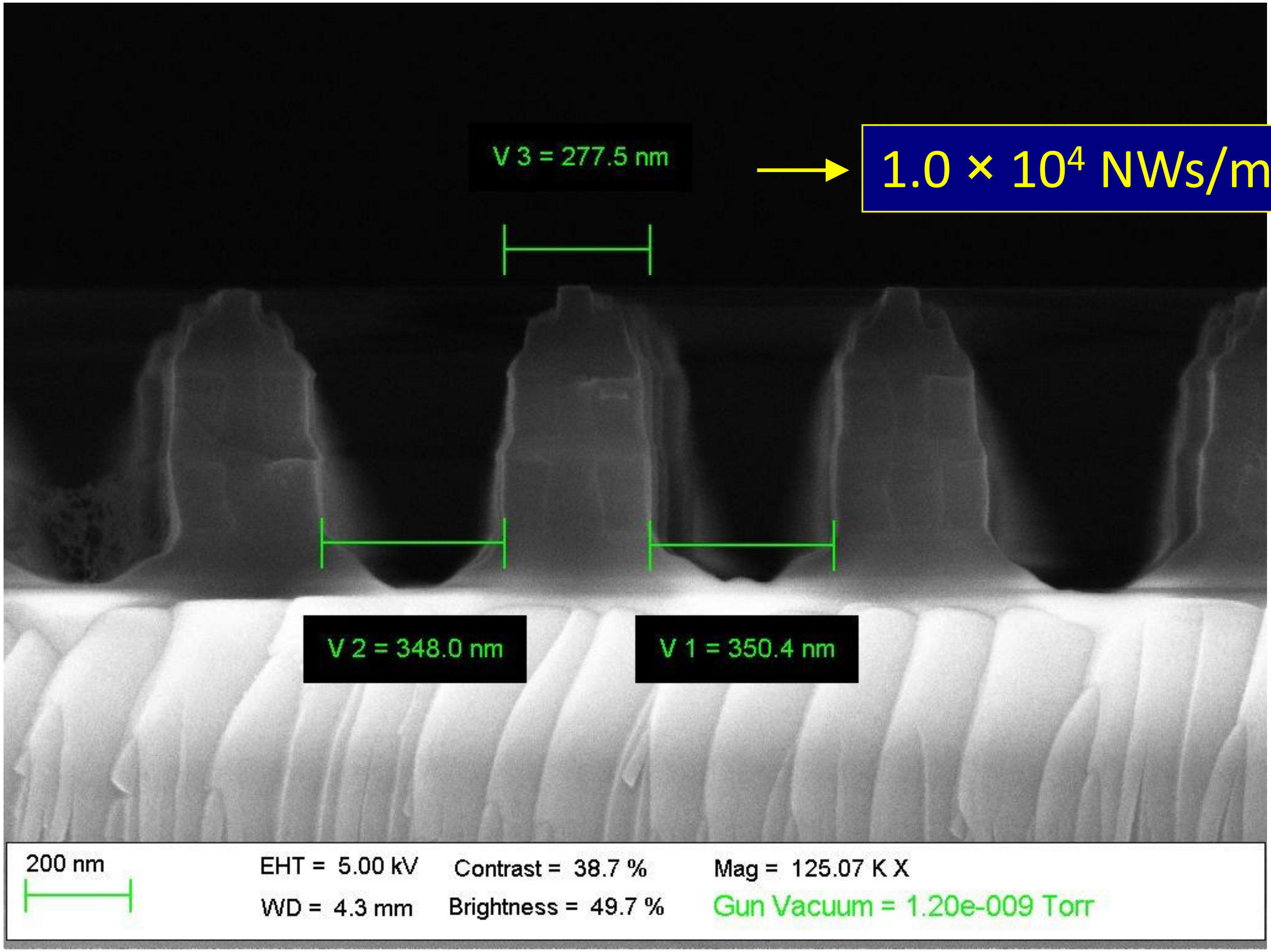


Requirements for high-performance top-down TEGs

From simulation results, the following requirements have been derived for high-performance top-down TEGs:

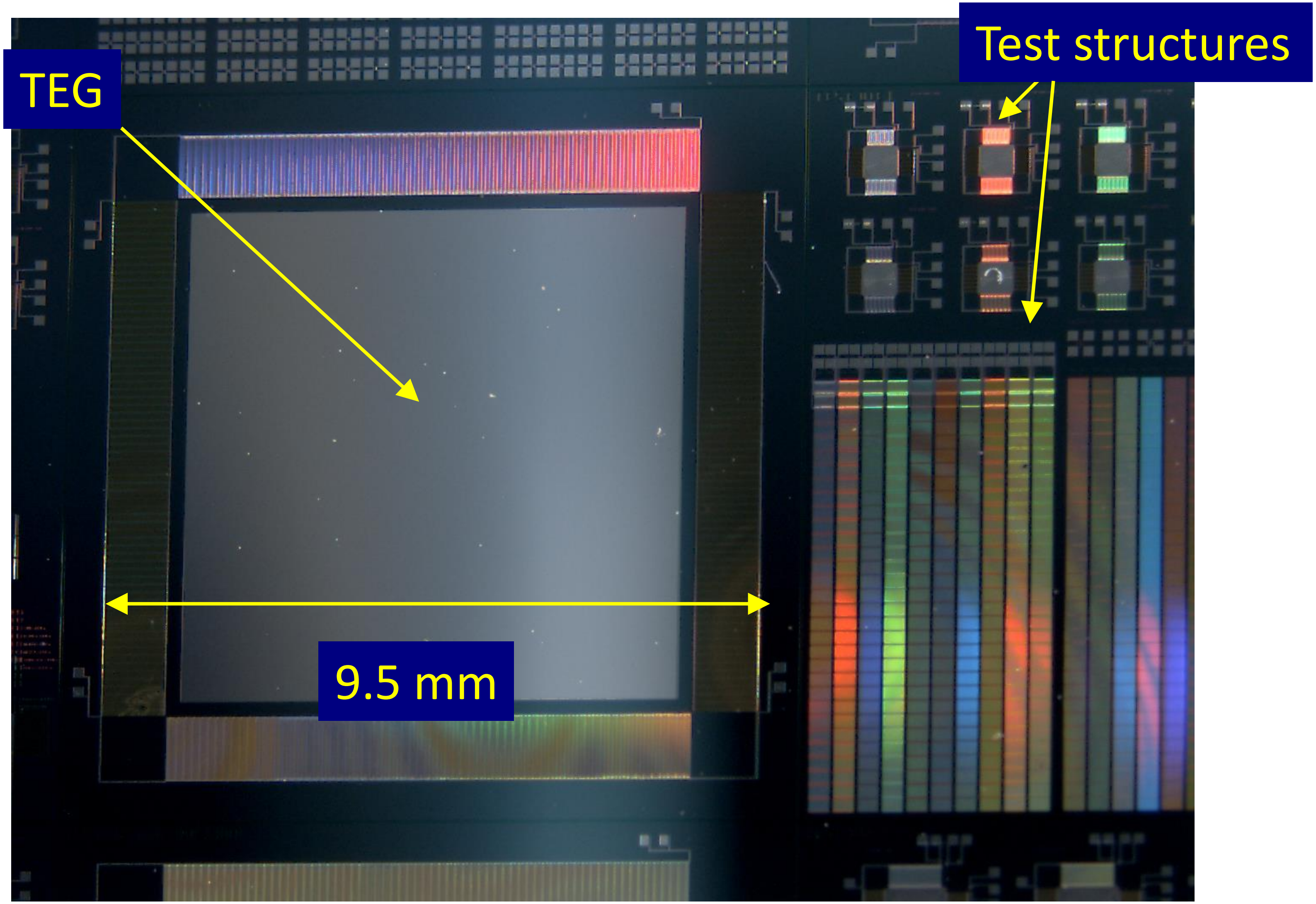
- Use of high density NWs arrays as thermoelements in the TEGs
- Fabrication of low resistivity NWs with n and p-type doping on the same substrate
- Vacuum packaging technology for the lateral TEGs, if possible, in order to eliminate heat exchange through air
- Fabrication of TEGs with a large number of thermocouples in series in order to multiply the output voltage (important for readout)

Lateral TEG – High-density NWs

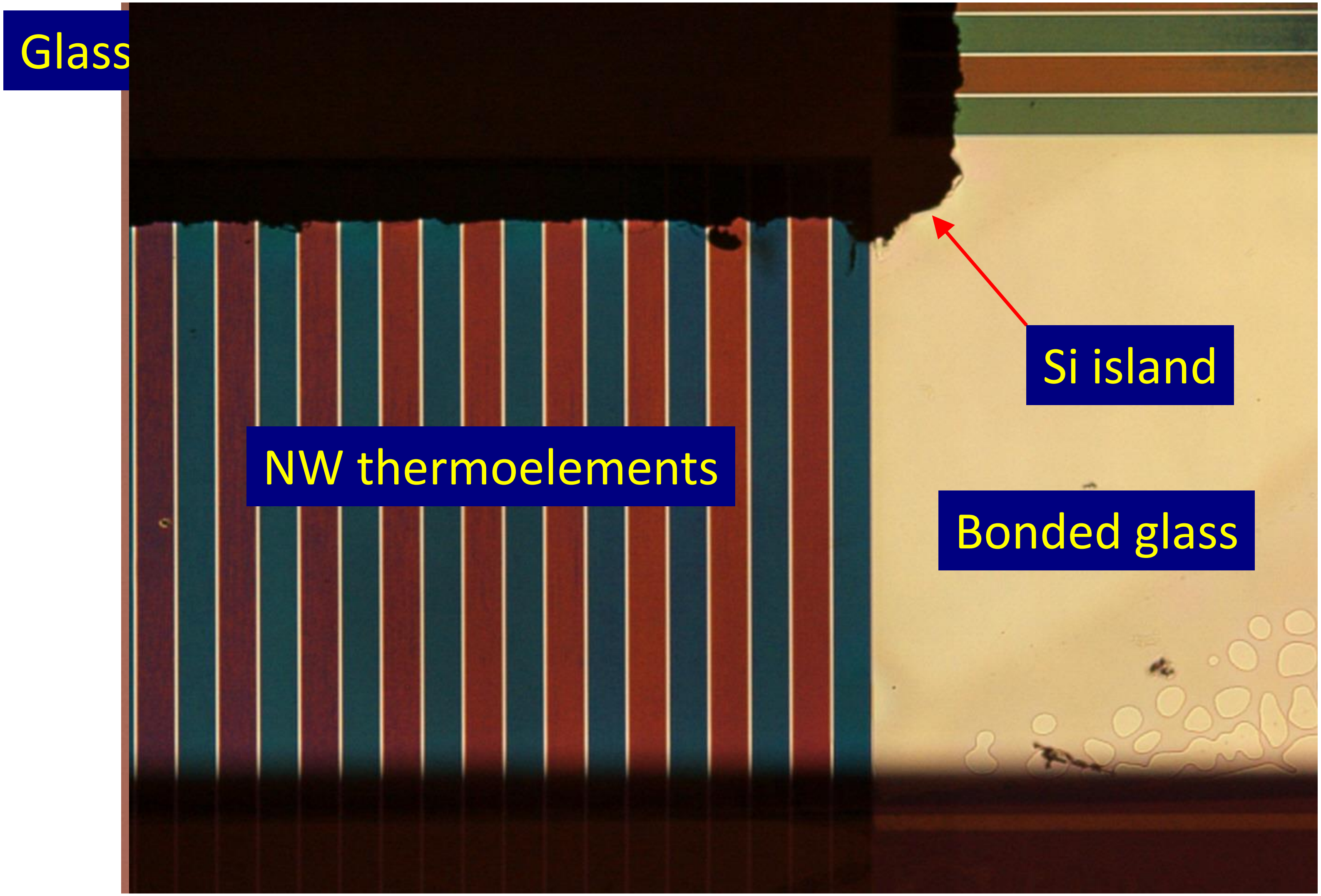


→ 1.0 × 10^4 NWs/mm

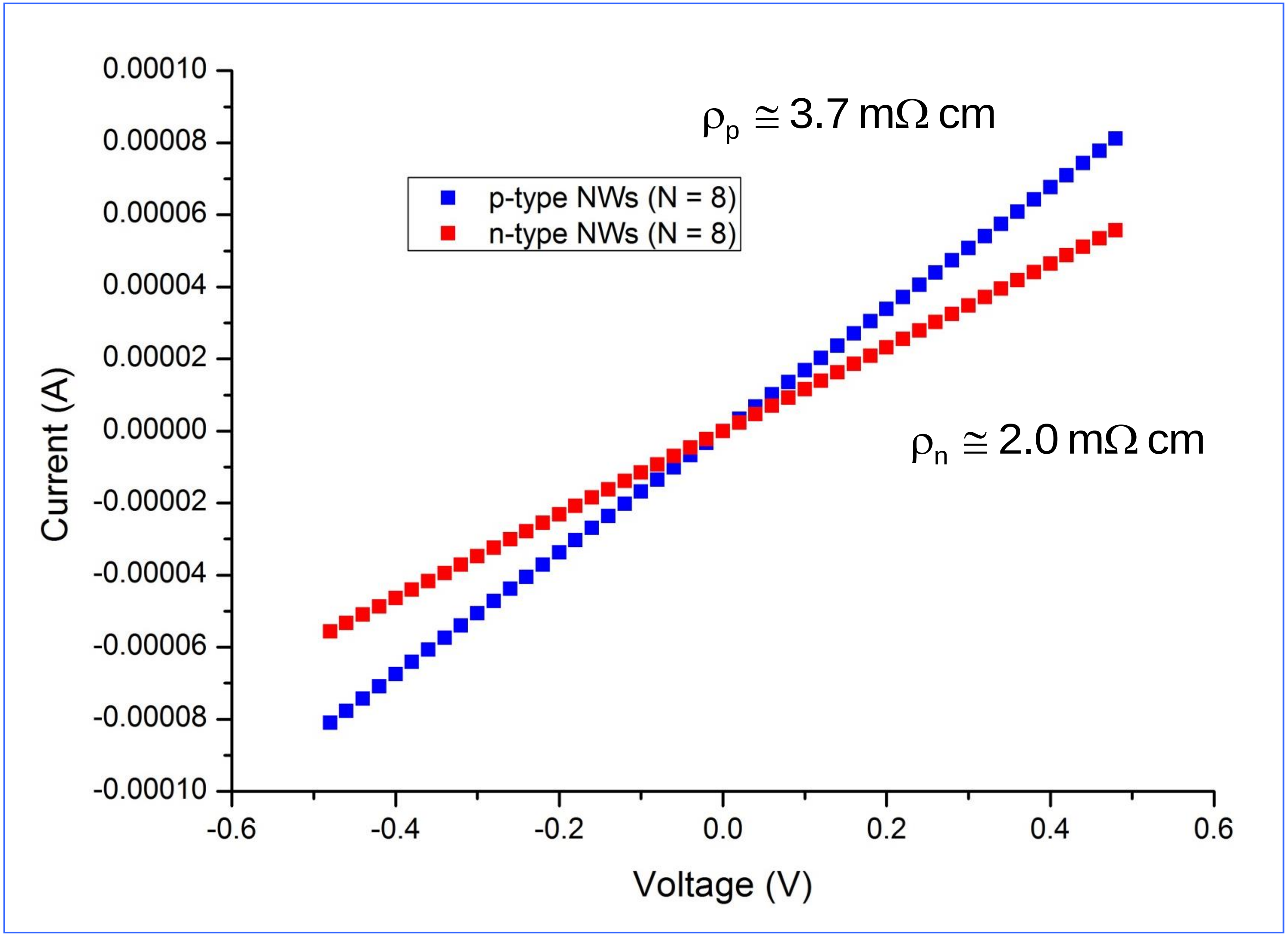
Lateral TEG – TEGs and test structures on the same wafer



Lateral TEG – TEGs and test structures in vacuum



Lateral TEG – IV measurements on NWs



$\rho_p \cong 3.7\ \mathrm{m\Omega\ cm}$

$\rho_n \cong 2.0\ \mathrm{m\Omega\ cm}$

Lateral TEG – Thermopiles composed by NWs