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Top-down and bottom-up approaches for SiNWs based micro-TEGs

Outline

- Why «all silicon» TEGs
- Demo applications
- Redundancy
- Thermoelectric generators:
  - bottom-up
  - top-down

Why microenergy solutions: Replace primary batteries (cost, environmental, deployment flexibility issues) by harvesters + secondary batteries

Why Silicon materials and architectures: tap into the micro-nanoelectronics field which is an enabling technology, dealing with miniaturised and high density features (3D) implementations, offering economy of scale (serve mass markets) and the possibility of integration and addition of control and smartness

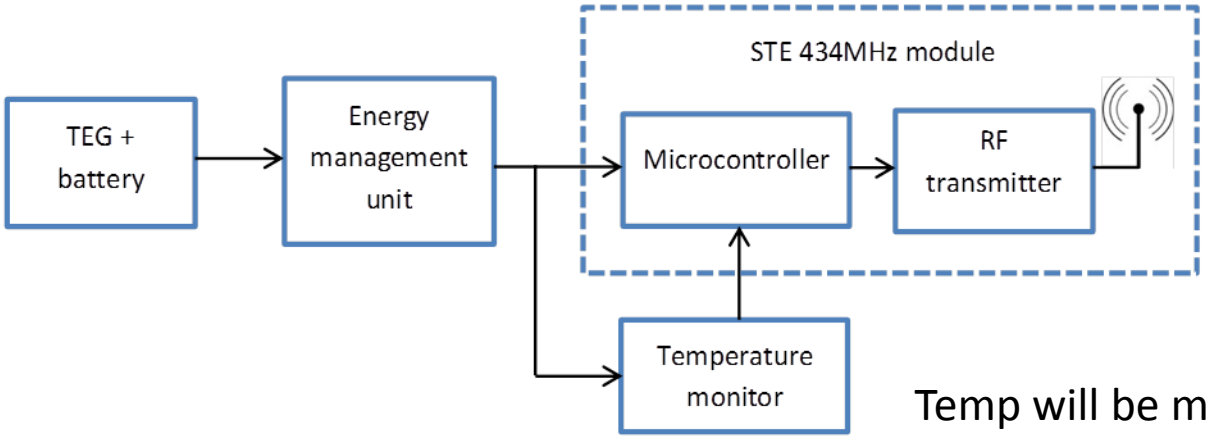
Why such applications: complementary microenergy testbeds from the perspective of silicon benefits ('smaller is better', 'cheaper is better') and availability of energy harvesting sources

Application scenario: Industrial Fryers

Industrial fryers are gas-powered, unplugged industrial appliances.

EC regulations require oil quality to be monitored. A log of oil temperature vs. time would fulfil this obligation.

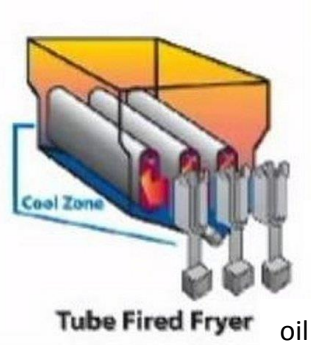
Thermal harvester will supply the power needed to monitor oil temp and to transmit data through a wireless connection to a remote data logging system without the burden of wiring the fryer to the electric net.

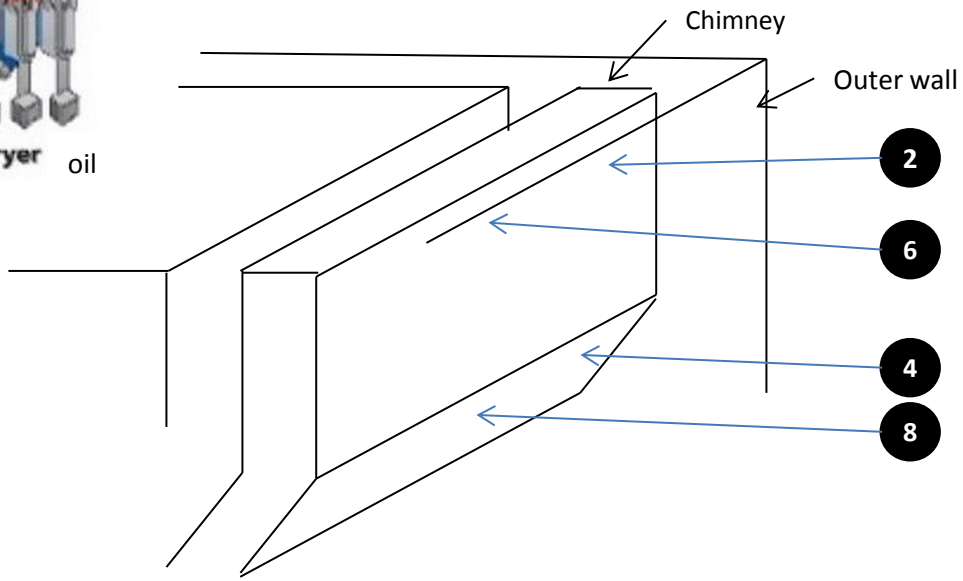


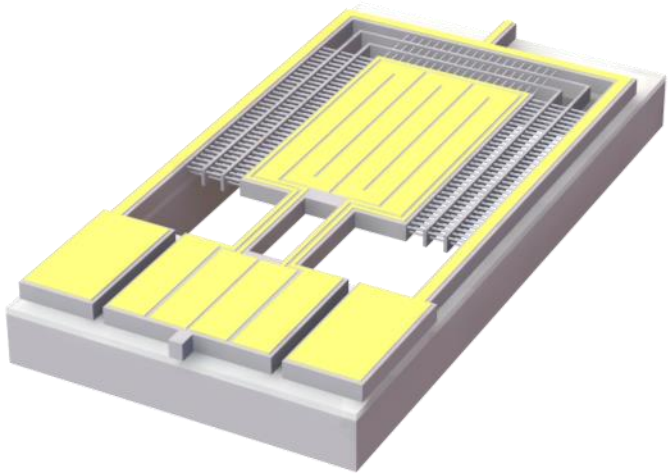
Temp will be monitored using TCs directly connected to the microcontroller

Application scenario: Industrial Fryers

Hot and cold spots needed to thermal harvesters were located at chimney walls.

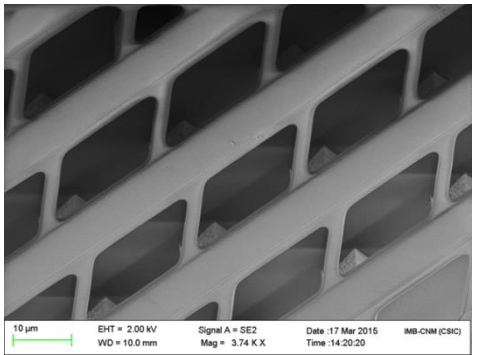






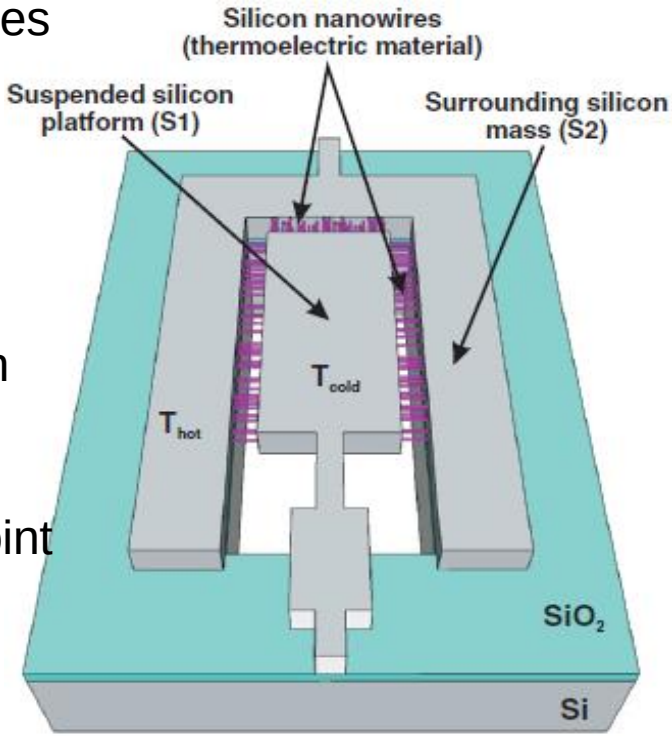
CSIC (Barcelona) and IREC (Barcelona)

THE BOTTOM UP STRATEGY



Bottom-up strategy – The material

- Deposition of gold nanoparticles on device trenches by Galvanic Displacement
- Growth of silicon nanowires on CVD by VLS synthesis
- Removal of membrane and passivation oxide with HF
- Drying of the device with nanowires by Critical Point Drying/Freeze Drying



Dávila et al, J. Elect. Mat., Vol. 40, No. 5, 2011

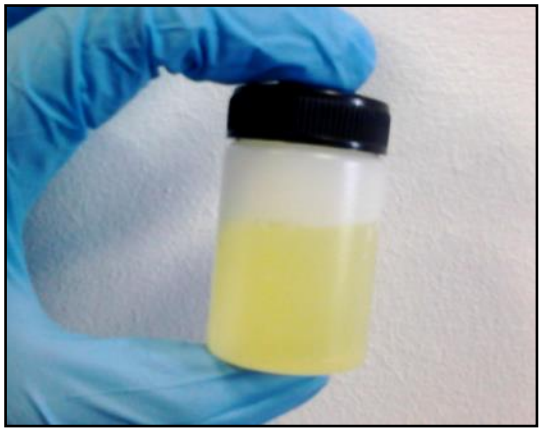
Microemulsion Galvanic Displacement

1 – **Microemulsions** are **prepared**.

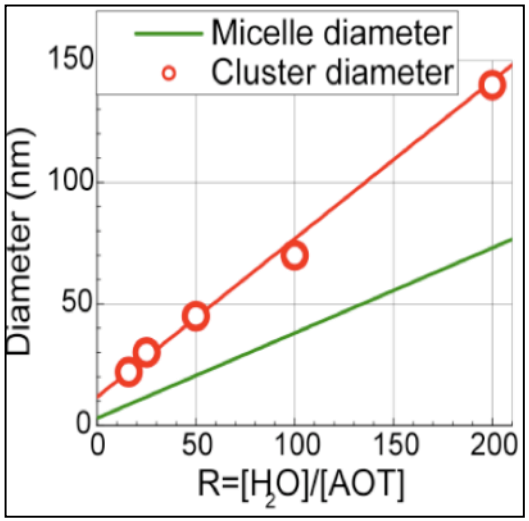
Aqueous phase: 0.2M HF + 0.01M $KAuCl_4$

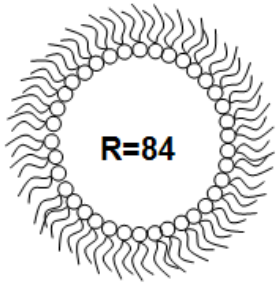
+

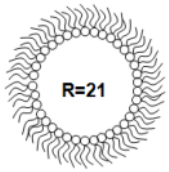
Organic phase: 0.33M AOT (surfactant) in n-heptane

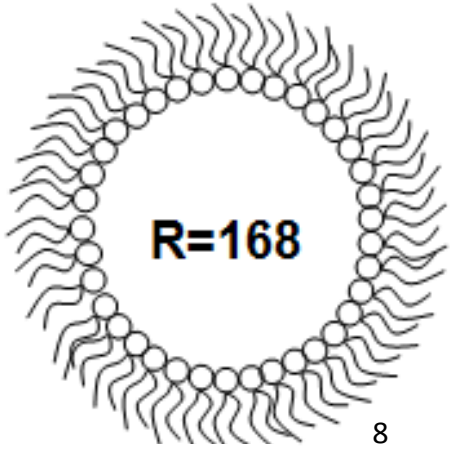


$$R = \frac{[\text{Water}]}{[\text{Surfactant}]} = \frac{[H_2O]}{[AOT]}$$









Gao et al, J. Am. Chem. Soc. 127, 4574 (2005)

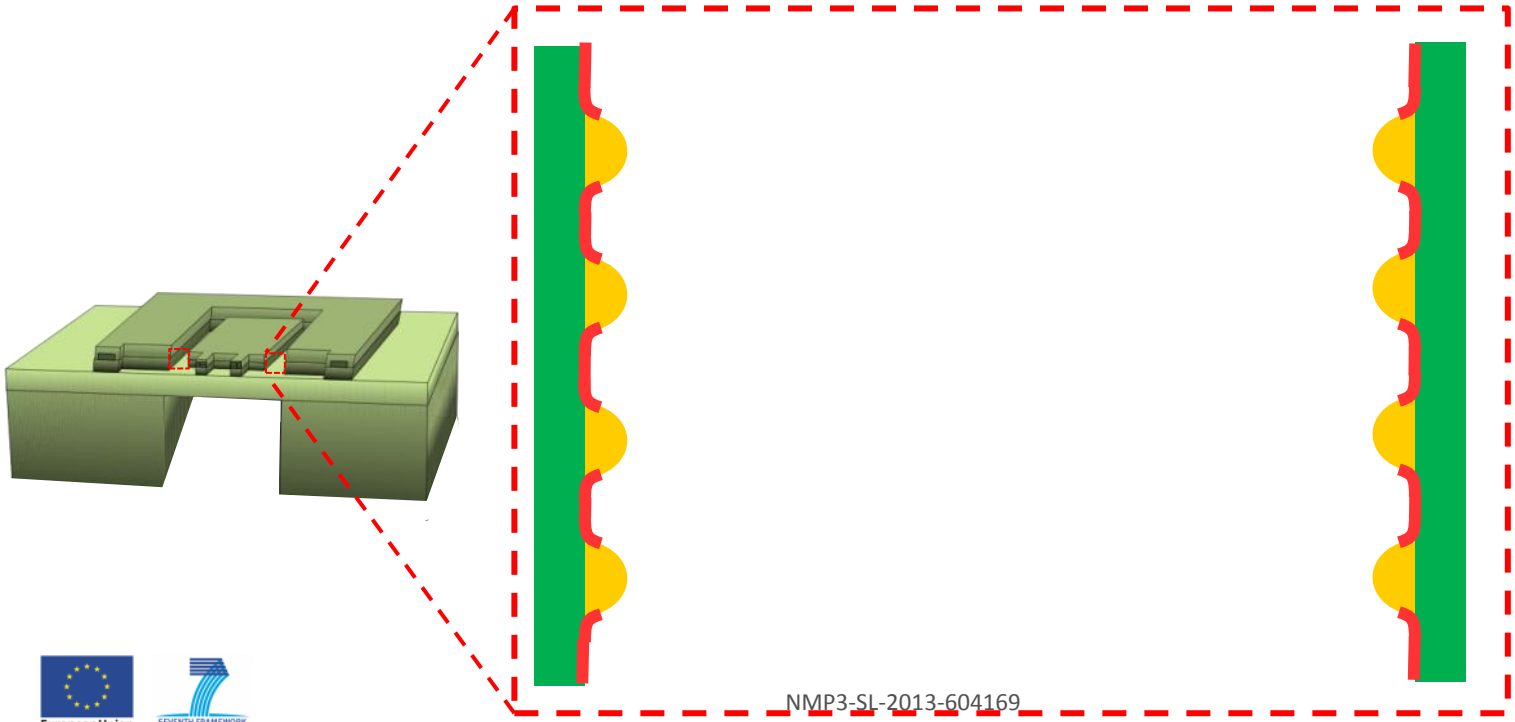
Microemulsion Galvanic Displacement

1 – Several **microemulsions** with different R values are **prepared**.

2 – Devices are **dipped in HF** in order to remove native oxide from trenches

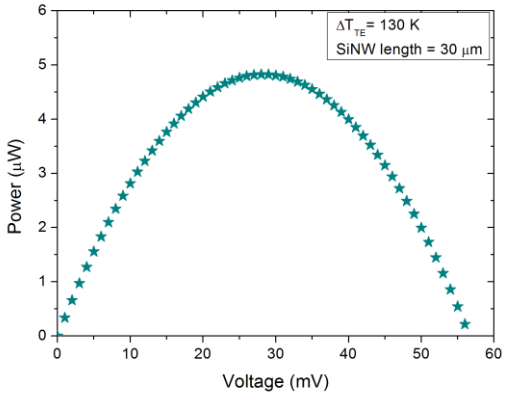
3 – Devices are **dipped in microemulsions** during a controlled dipping time. Gold NPs are formed

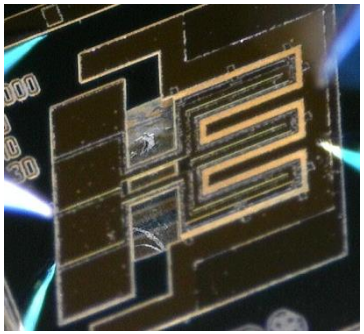
4 – Devices are **annealed** to remove the remaining surfactant



μTEG basic characterization – IV curve

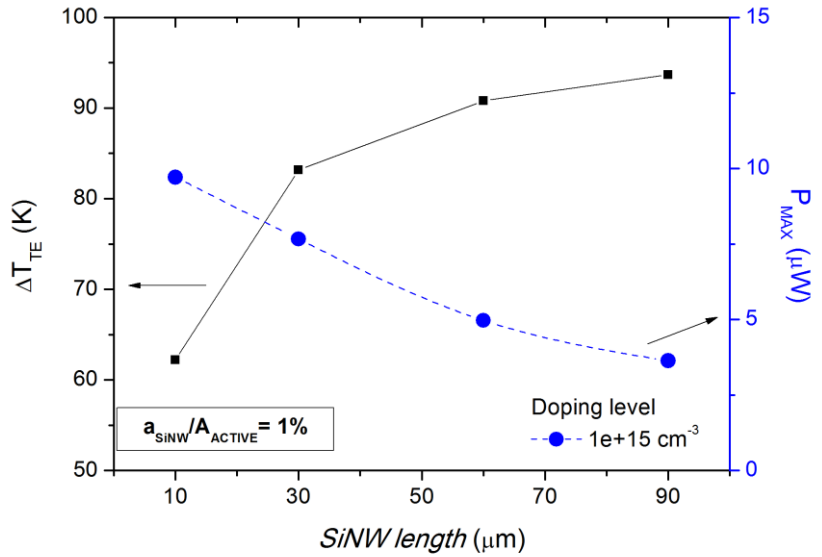
Real device under test mode



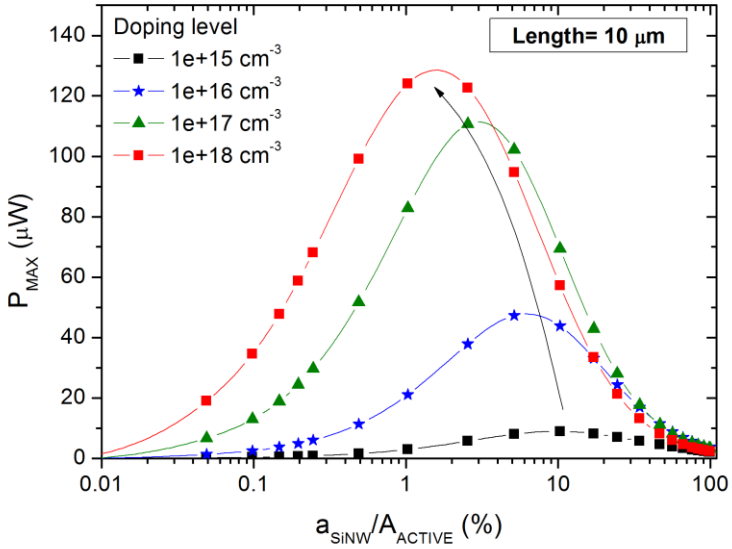


Parameter	Value
S_{SiNW}	1.46e-3 V/K
ρ_{SiNW}	13.5 Ωcm
k_{SiNW}	50 W/mK
L_{SiNW}	10 - 90 μm
$r_{AMBIENT}$	76.4 K/W
R_{PATH}	50 Ω
ΔT_{TE}	100 K

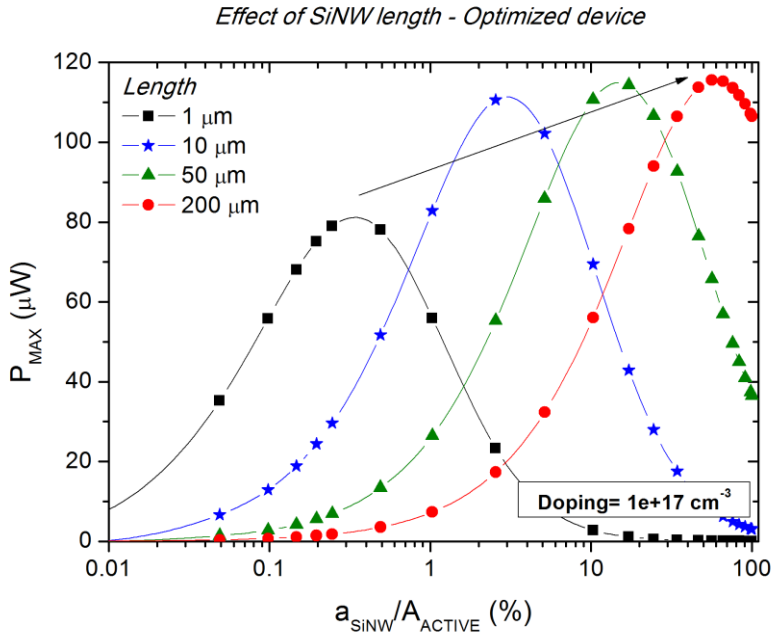
Effect of low doping level of SiNW - Non-optimized device



Effect of SiNW doping level - Optimized device



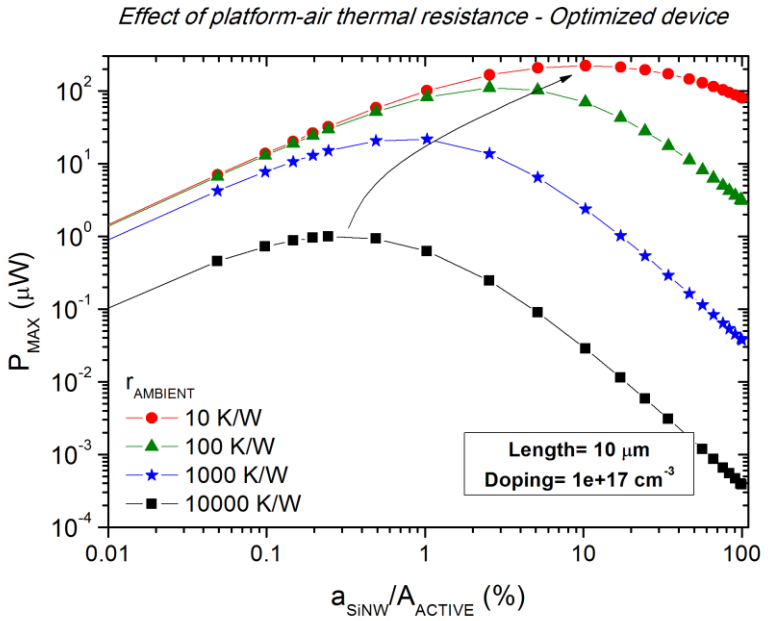
μTEG basic characterization – IV curve



ining the device I-V curve

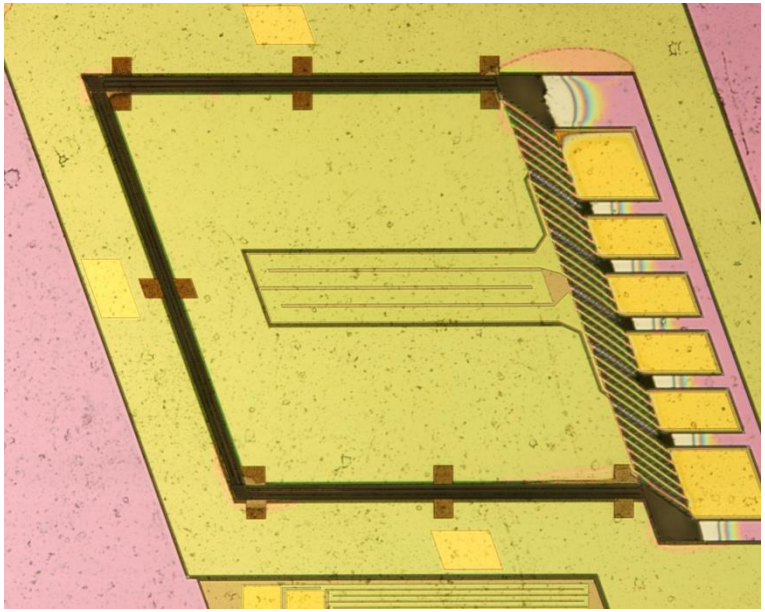
Doping level effect on device performance

SiNW density effect on device performance



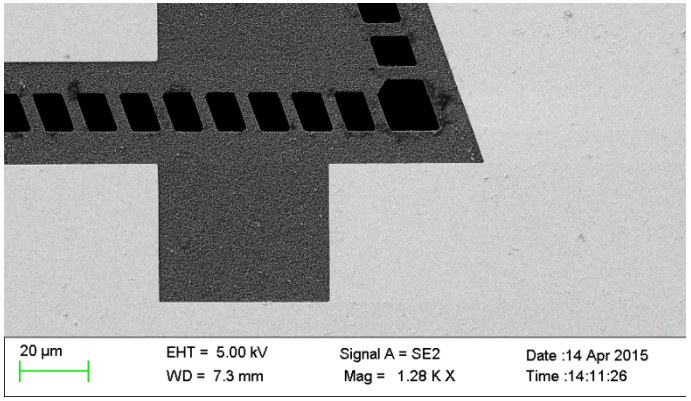
Bottom-up strategy – Si platforms

- Multiple configurations, for pure harvesting or test purposes, with built-in heaters for characterization with controlled gradients.

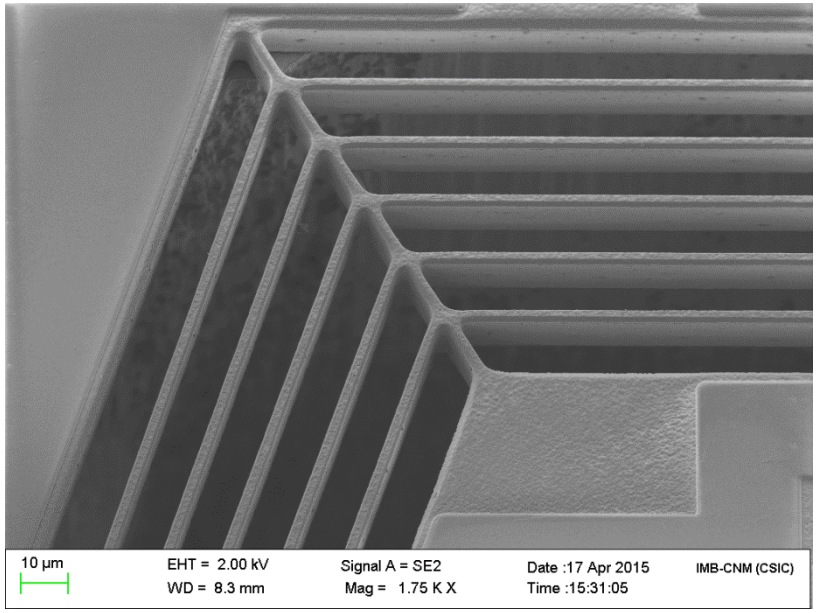


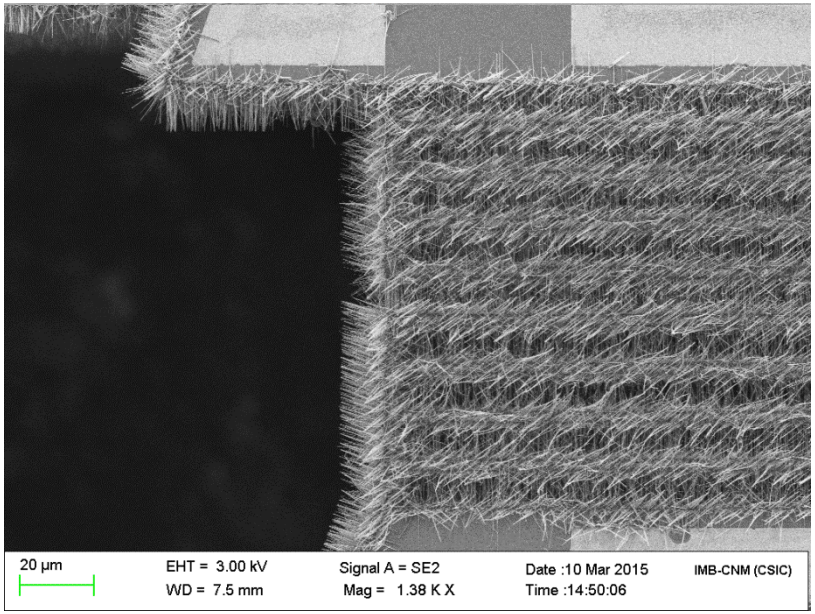
- Series and parallel connections of multiple devices.

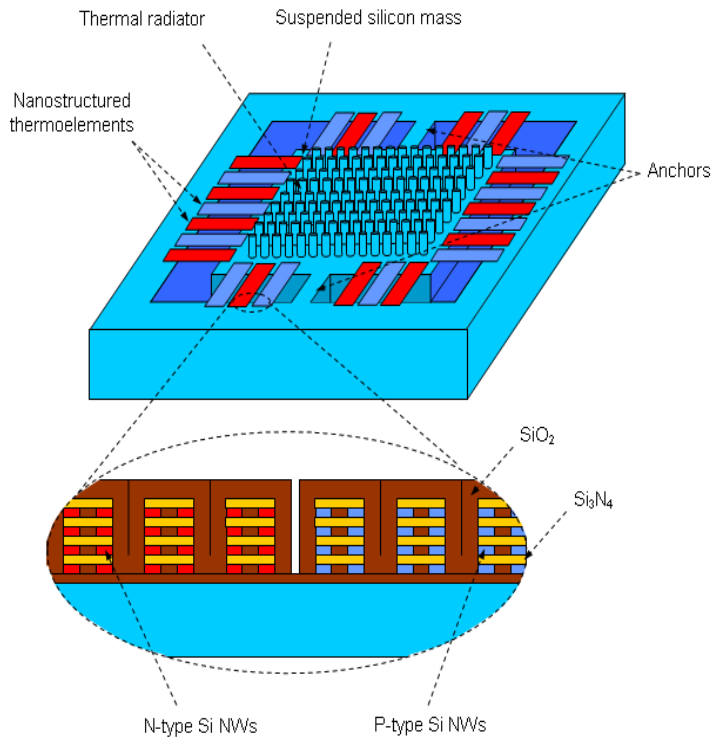
- different length of membranes.
- different numbers of trenches (1 to 4) to be filled by Si NWs.
- bridges in place of membranes.
- no temporary Si bulk supports.
- prefixed percentages of bulk Si.



Bottom-up strategy – Si platforms







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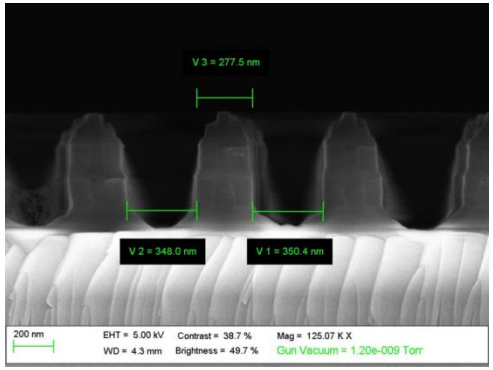
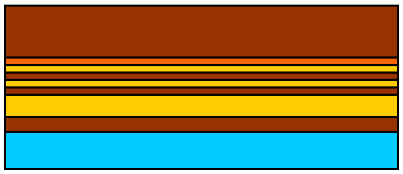
THE TOP-DOWN APPROACH



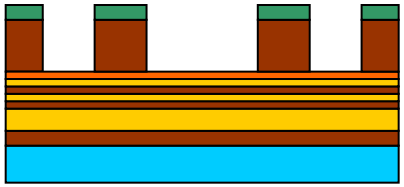
Lateral TEG - process flow (1)

1. Bulk Si

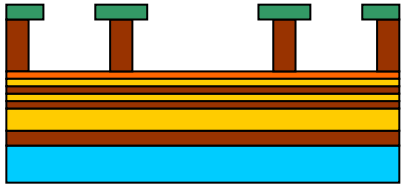
2. SiO_2/Si_3N_4/poly deposition



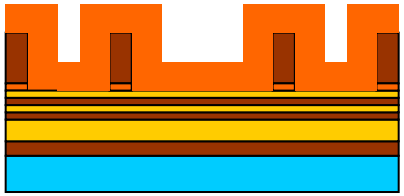
3. SiO_2 RIE



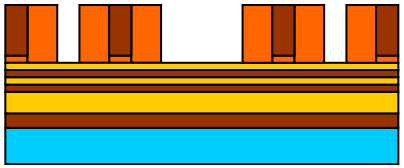
4. SiO_2 wet etching



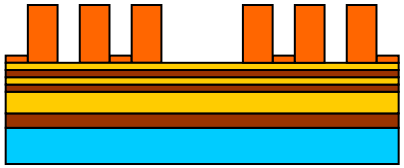
5. Poly deposition



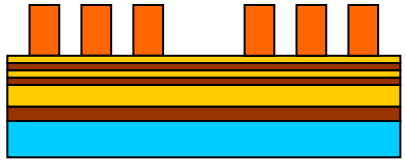
6. Poly RIE



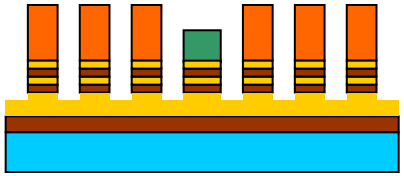
7. SiO_2 wet etching



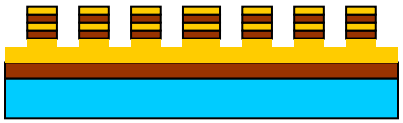
8. Poly RIE



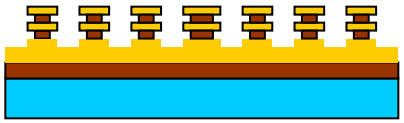
9. SiO_2/Si_3N_4 RIE



10. Poly wet etching



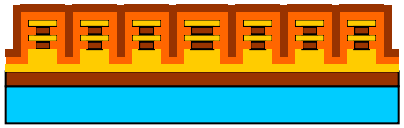
11. SiO_2 wet etching



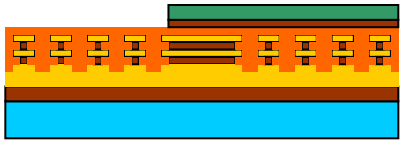
12. Poly deposition

Lateral TEG - process flow (2)

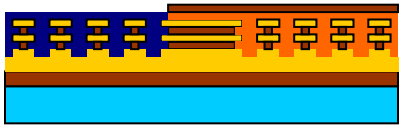
13. SiO_2 deposition



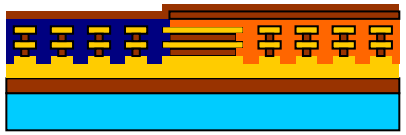
14. SiO_2 wet etching



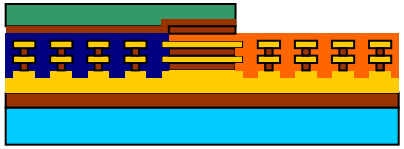
15. P-type doping



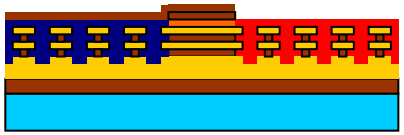
16. SiO_2 deposition



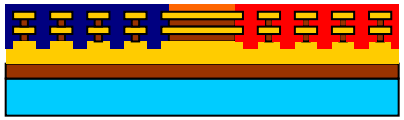
17. SiO_2 wet etching



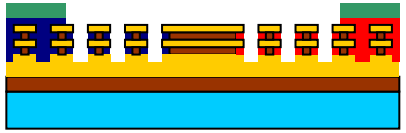
18. N-type doping



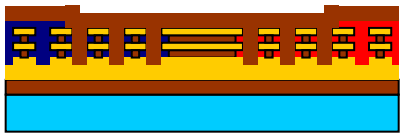
19. SiO_2 wet etching



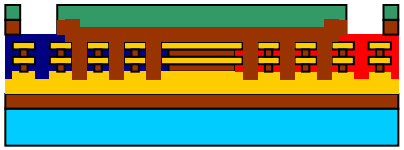
20. Poly RIE



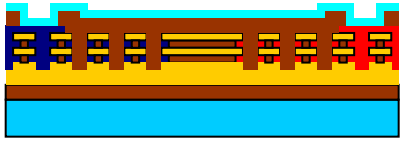
21. SiO_2 deposition



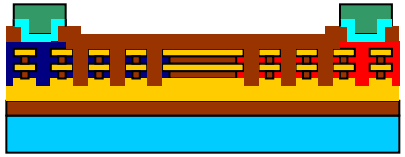
22. SiO_2 wet etching



23. Al/Si deposition

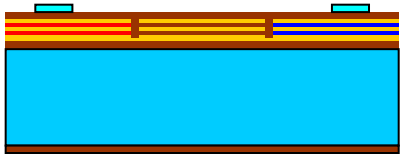


24. Al/Si etching

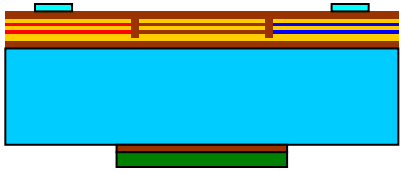


Lateral TEG - process flow (3)

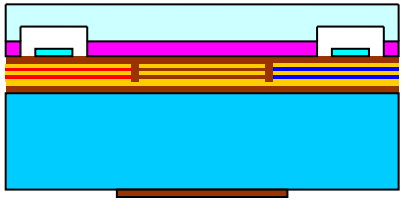
25. Wafer with NWs



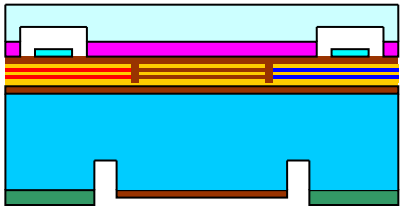
26. SiO_2/Si_3N_4 RIE



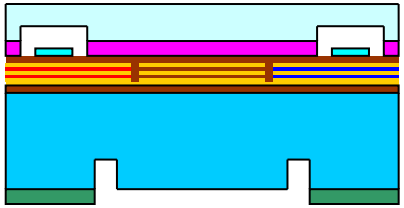
27. Wafer bonding



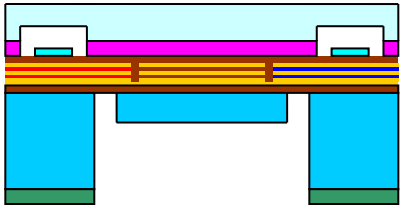
28. Si DRIE



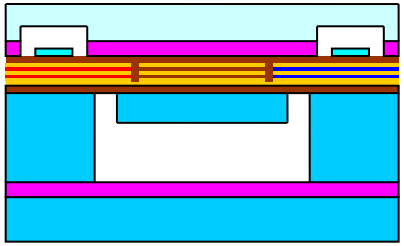
29. SiO_2 etching



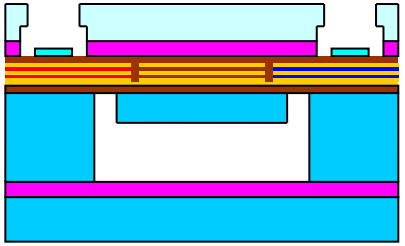
30. Si DRIE



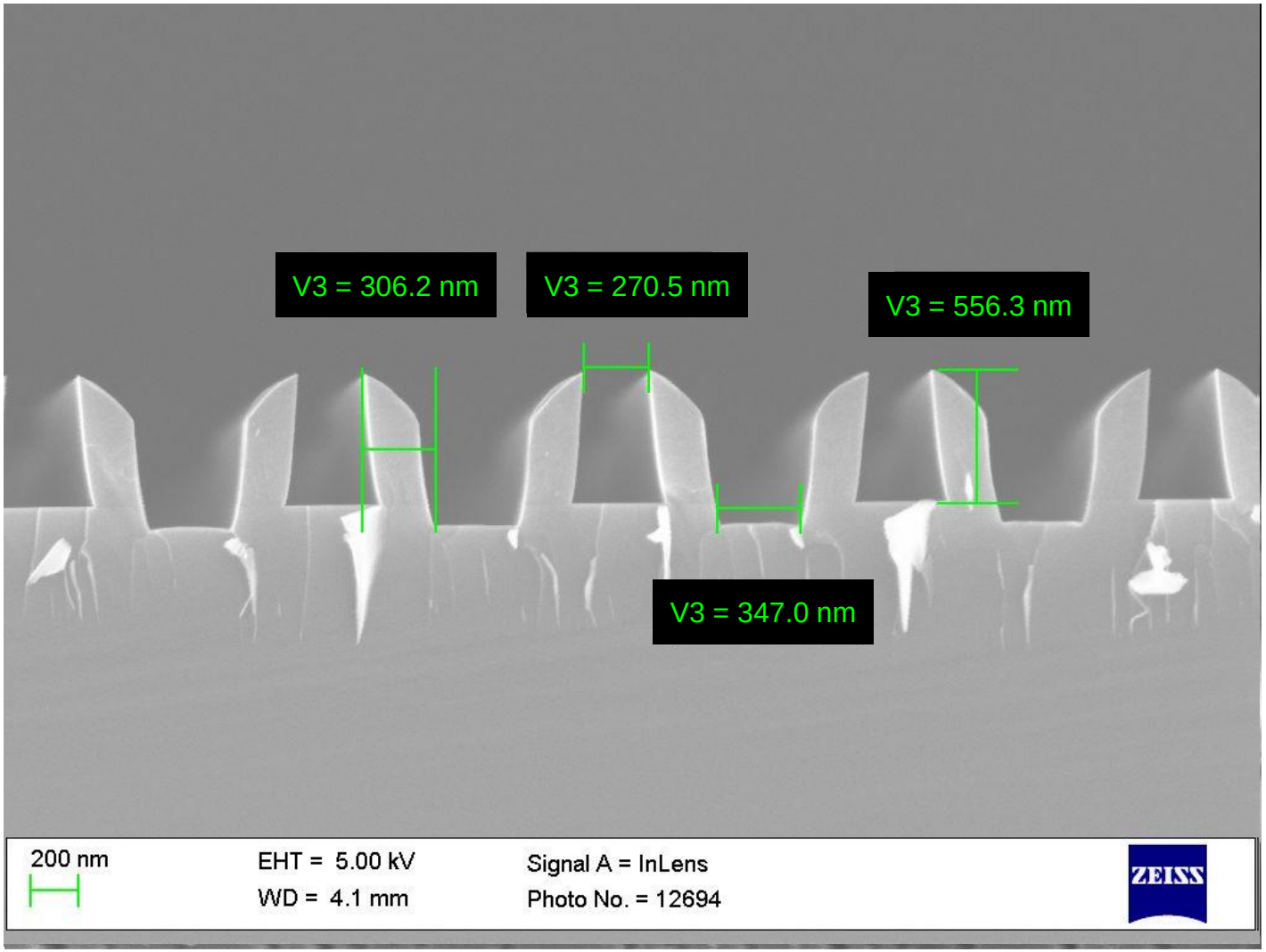
31. Wafer bonding



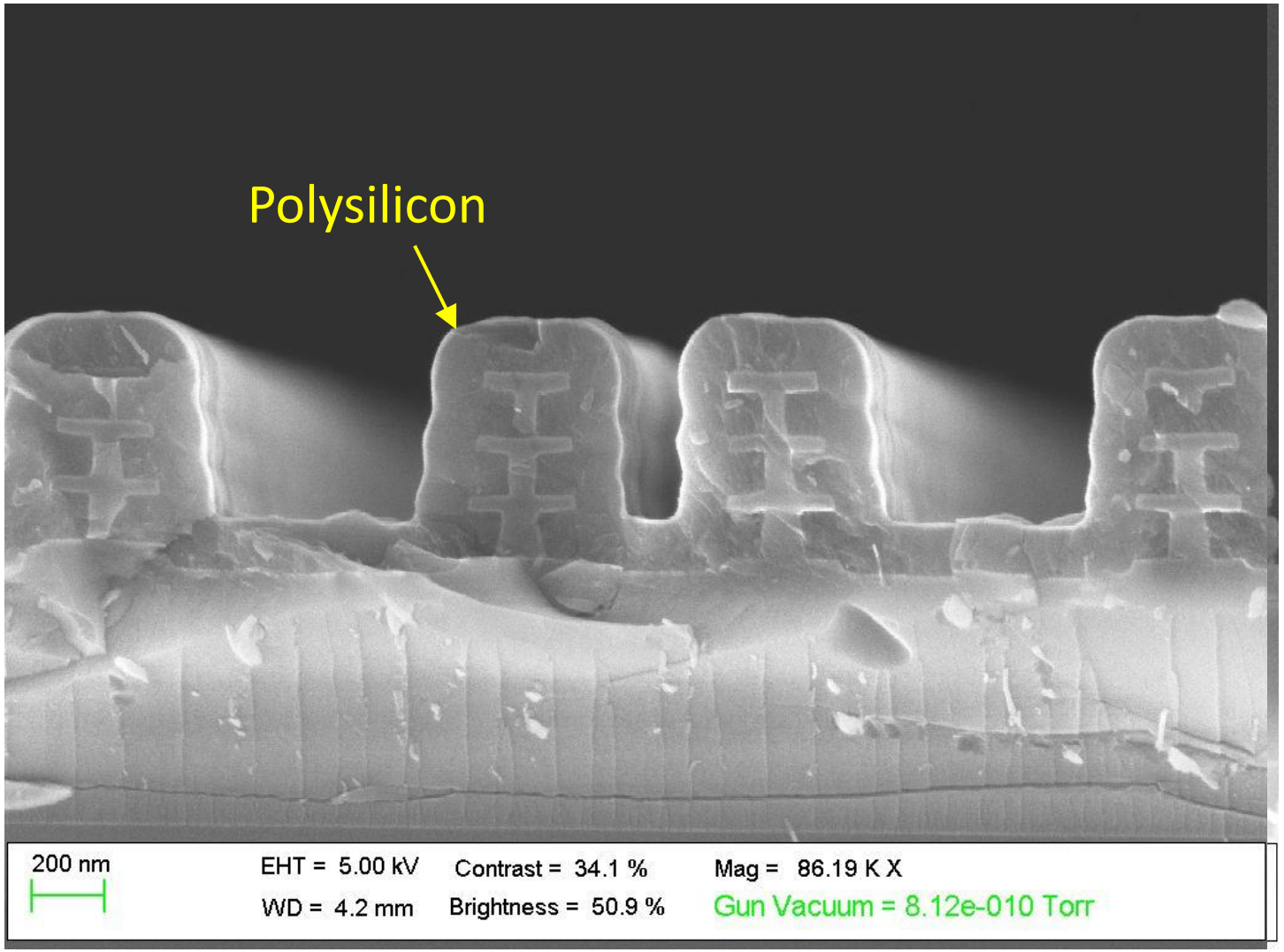
32. Glass dicing



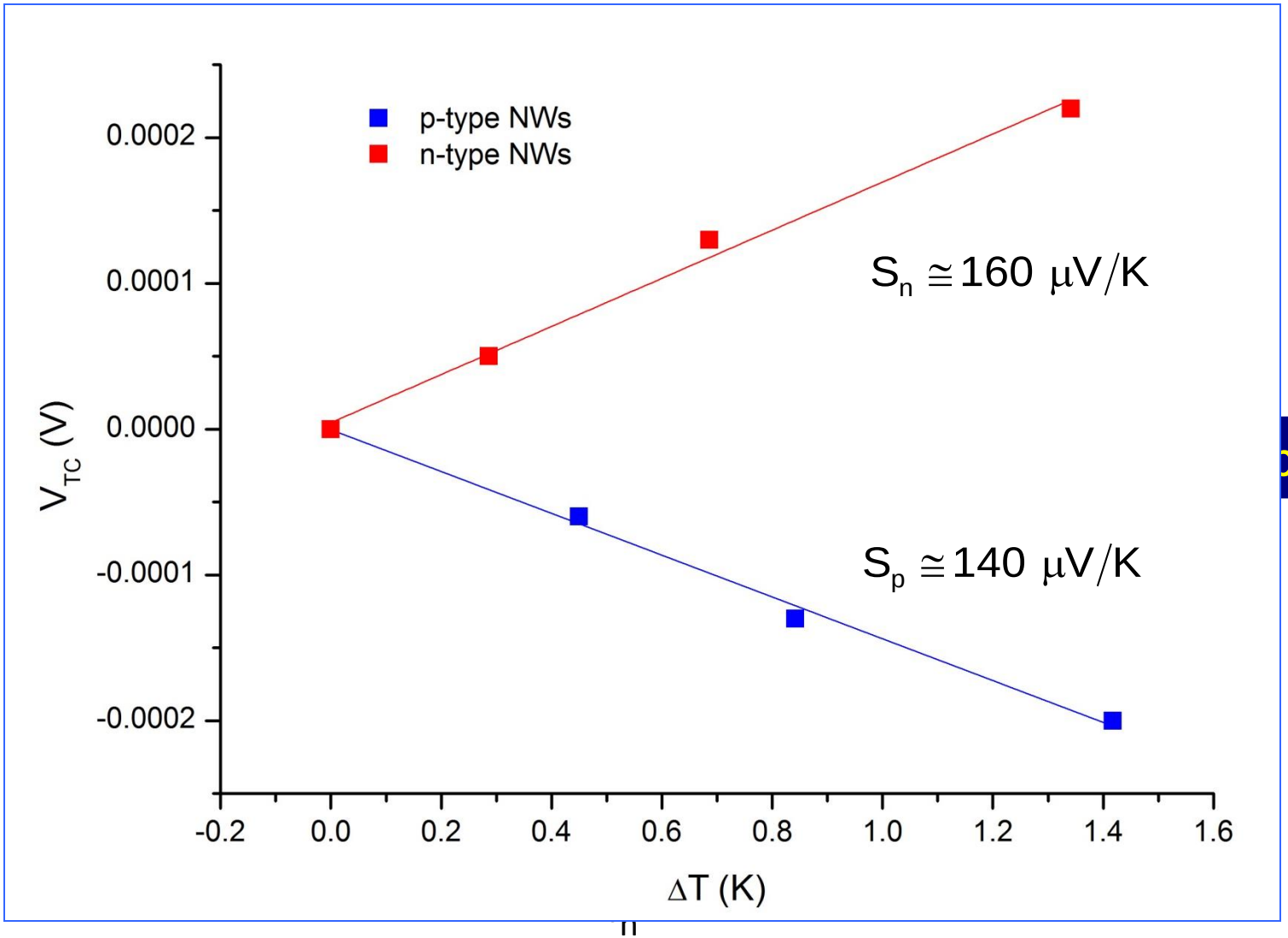
Lateral TEG – Spacers for high-density NWs



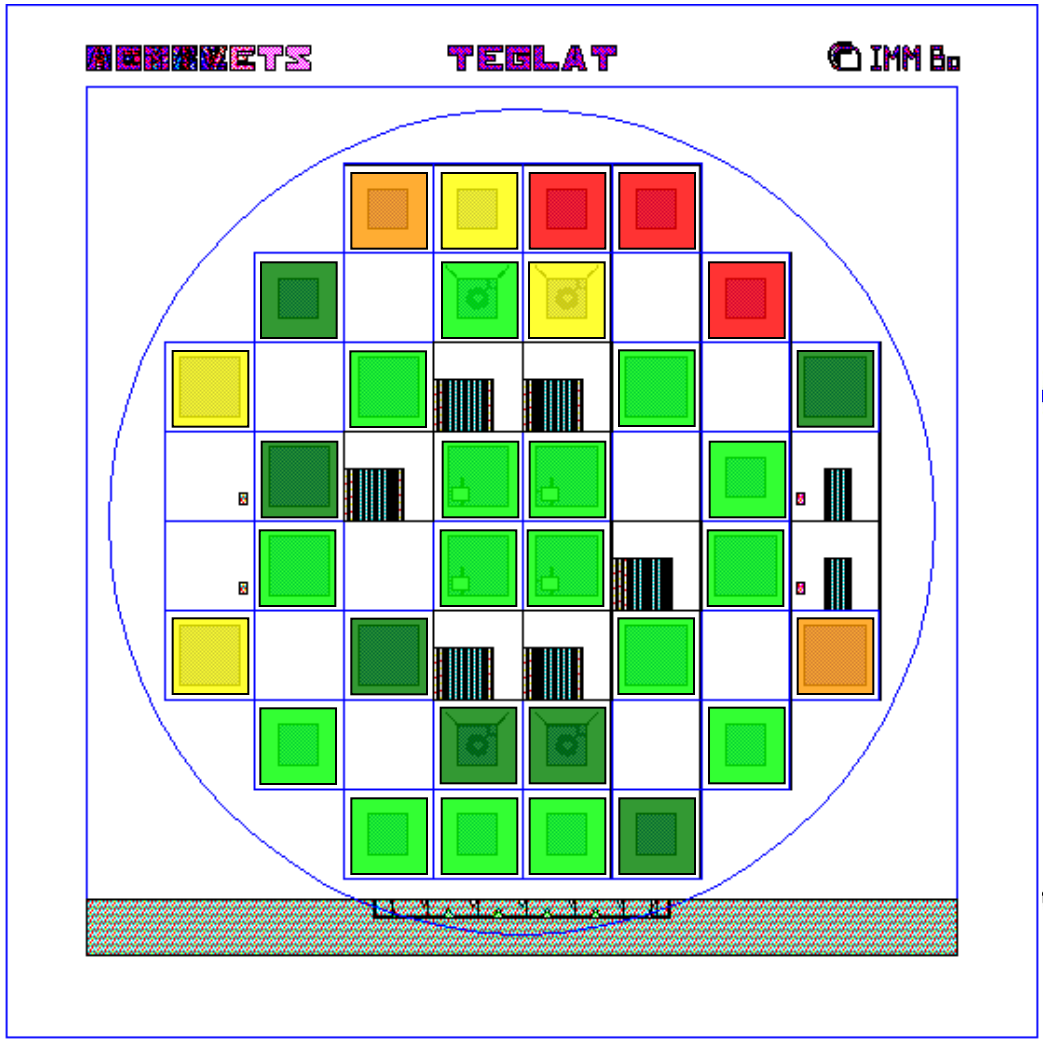
Lateral TEG – SiO_2/Si_3N_4 templates for NWs



Lateral TEG – Seebeck measurements on NWs



Lateral TEG – Yield test on TEG prototypes



256 Thermocouples in series

Fully functional device

3 working sides

2 working sides

1 working side

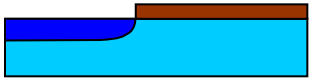
0 working sides

5 10

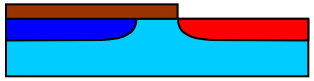
Vertical TEG – Process flow

1. Si substrate

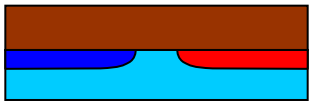
2. P-type doping



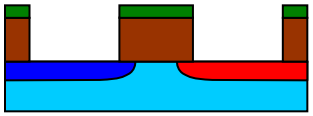
3. N-type doping



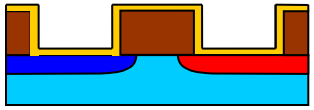
4. Thick SiO_2 deposition



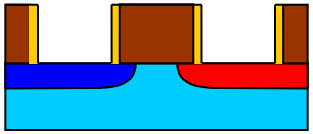
5. SiO_2 RIE



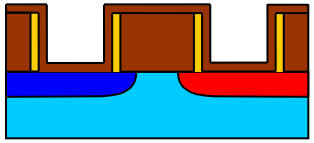
6. Si_3N_4 deposition



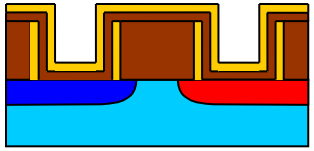
7. Si_3N_4 etchback



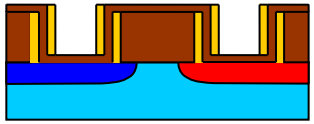
8. SiO_2 deposition



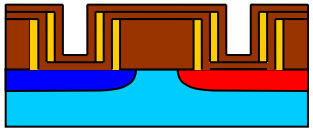
9. Si_3N_4 deposition



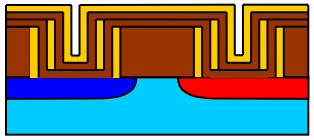
10. Si_3N_4 etchback



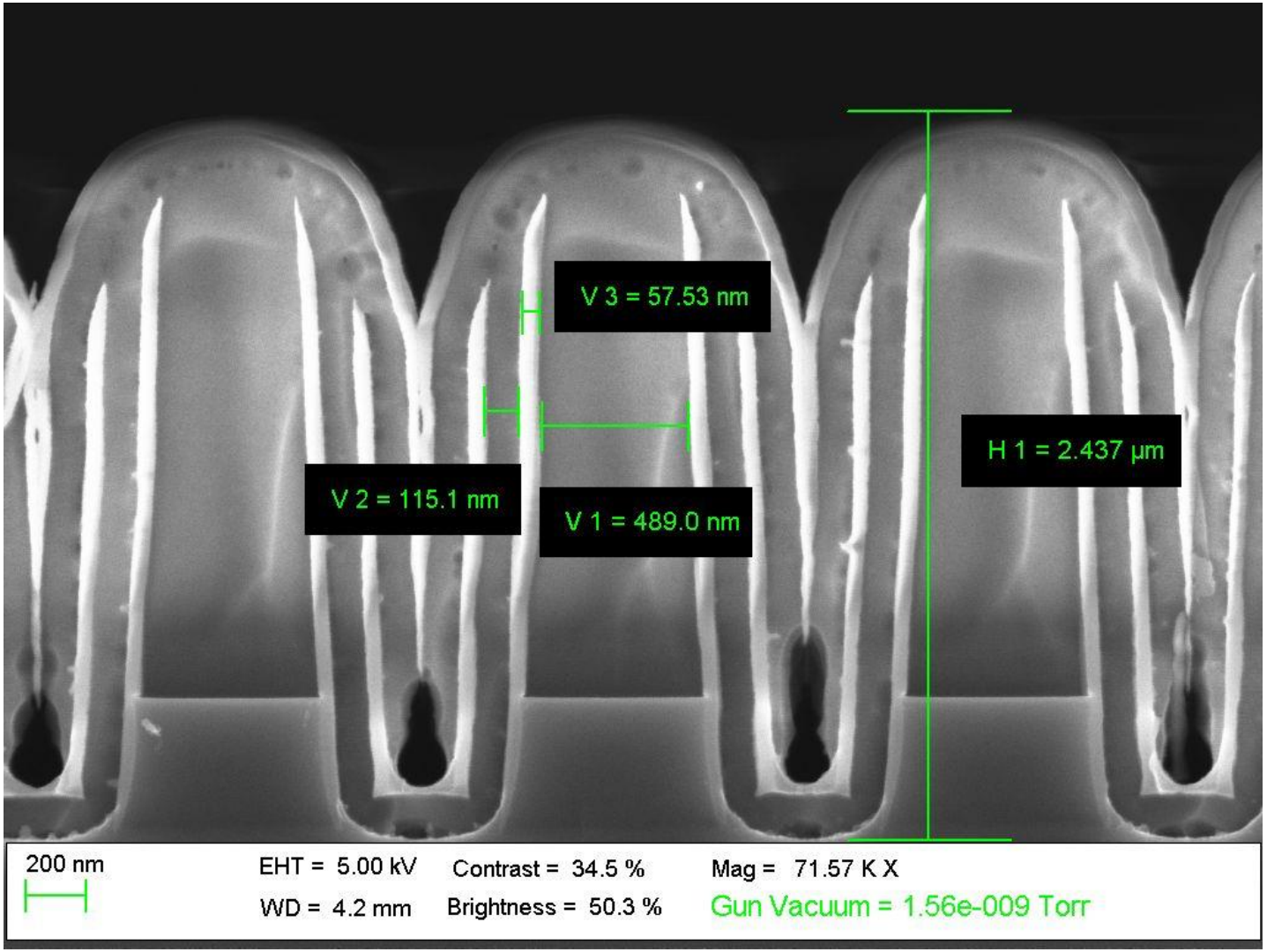
11. SiO_2 deposition



12. Si_3N_4 deposition



Vertical TEG–SiO_2/Si_3N_4 templates for high-density NWs



Summary

- Lateral NW arrays with linear density of 1.0×10^4/mm have been obtained.
- On the high-density lateral NWs, electrical resistivity values around 2.0 mΩ cm with n-type doping and 4.0 mΩ cm with p-type doping have been achieved.
- The measured Seebeck coefficient was around 150 μV/K for both doping types.
- An overall functionality above 80% has been obtained on lateral TEG prototypes in yield tests.
- The fabrication of vertical TEGs is ongoing. Early results on the fabrication of high-density templates for vertical NWS have been obtained.

Conclusions

- Both top-down and bottom-up approaches to TEGs could achieve their target as of nominally available power density.
- Next targets of WP2 will be
  - assembling and wiring the chips
  - packaging
  - testing (benchtop, simulated, and actual scenario)

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