Smart integration of Si NWs arrays in all-silicon thermoelectric micronanogenerators

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Abstract

In order to fulfill new paradigms such as *Internet of Things* or *Trillion Sensors* large volume fabrication of miniaturized devices need to be considered. In order to provide those devices with energy autonomy, solutions other than primary batteries, i.e. energy harvesting approaches, are advisable. In those scenarios where residual heat is present thermoelectricity may be explored as a source of energy autonomy. Miniaturization and large volume fabrication are characteristics of Silicon technologies. Although thermoelectric materials tend to be semiconductors, silicon itself is not a good candidate in bulk form due to its high thermal conductivity. However, it was predicted (and lately experimentally confirmed) that silicon in nanowire form (Si NWs) could increase its inherent thermoelectric figure of merit by two orders of magnitude. This interesting piece of information was gathered by painstakingly placing a single nanowire (grown elsewhere and sonicated) in a suspended thermal microstructure and securing its mechanical and electrical bonds by means of FIB-assisted processes. It is obvious that to fabricate a useful thermoelectric device much more *populated arrays* of Si NWs need to be integrated in a way that their mechanical and electrical connections to the active parts of the generator are achieved in a more *automated* way. Monolithic top-down approaches have been already assayed to achieve this goal with silicon technologies. For instance, a planar microgenerator can be obtained by fabricating a suspended silicon platform and defining a low density Si NWs array in a SOI wafer with a nano-thick device layer. The resulting devices are fragile and require the use of time-consuming nanopatterning techniques such as e-beam or FIB. A second approach is using state of the art submicron CMOS technologies to obtain more robust structures and higher density arrays of Si NWs. In this case the microgenerator is of vertical architecture, which adapts better to naturally occurring thermal gradients, but the ‘height’ of the vertically defined nanowires is limited to the order of one micron, which is not large enough to develop significant temperature differences across them.

In this work, two alternative approaches are introduced for automatically integrating large numbers of several microns long Si NWs in lateral thermoelectric devices. The devices

obtained and their electric and thermoelectric characterization will be presented. Both cases being planar require a thermally isolated platform to be defined by silicon micromachining. In this way the external vertical thermal gradients are transposed laterally into a structure consisting of a suspended platform (usually in contact with a heater exchanger) connected via Si NWs with the surrounding silicon bulk rim (usually in contact with the heat source).

The first approach provides a way to integrate medium-high densities of stacked top-down polysilicon nanowires. It makes use of multilayers of very thin silicon oxide and silicon nitride vertically patterned. A silicon oxide wet etch is performed to produce lateral nano-recesses in the oxide layers of the stacked structure. A conformal polysilicon deposition and dry etch-back follows, which fill-in the lateral nano-recesses giving rise to as long as designed polySi NWs arrays. Their section is roughly square, with a typical dimension of 70-100 nm. Linear densities of a few thousands of NWs per mm may be achieved without stressing much the finesse of the lithography.

The second approach shares with the previous one the use of top-down technology to produce the 3D platforms enabling areas of thermal contrast, but makes use of bottom-up techniques to obtain the massive parallel integration of nanoobjects. Higher densities can be thus obtained at a minimum technological cost since no fine lithography approach is needed. Si NWs are grown as a post-process in a SiH_4 based CVD process after a galvanic displacement method is used to selectively deposit gold nanoparticles in the vertical walls of the suspended platform and rim. The nanowires grow following the gold-assisted VLS (Vapor-Liquid-Solid) mechanism till they reach the opposing wall, bridging rim and platform. The NWs are connected quasi-epitaxially to both sides providing mechanically robust nanowire-bulk connections with very low thermal and electrical contact resistance. This approach produces Si NWs arrays of several nanowires per μm^2 with diameters in the 80-120 nm range. As in the previous case the nanowire length is governed by design. Since the growth of the NWs by CVD-VLS requires a (111) surface and a temperature of 650 ºC, the only precaution to be taken is the choice of the appropriate starting silicon orientation (100), the topographical alignment of the perimeters of platform and surrounding rim with the position of vertically occurring (111) planes, and the use of metals that can withstand the temperature of the CVD post-process.

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