Top-down fabrication of high density nanowire arrays for application in thermoelectric micro-energy conversion devices

- L.Belsito, F. Mancarella, A. Roncaglia.
- CNR-IMM, V. Gobetti, 101 - 40129 Bologna, Italy, belsito@bo.imm.cnr.it

Institute for Microelectronics and Microsystems (IMM), CNR (Italy)

SEVENTH FRAMEWORK PROGRAMME

SiNERGY

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Outline

- Requirement for high-performance thermoelectric generators (TEGs).
- Measurement of thermoelectric properties on silicon nanowires by nanomachined test structures.
- TEG based on Si NWs.
- Early test results on TEG prototypes.

TEGs with vacuum technology

- Second generation of TEG prototypes.
- Early test results.

TEGs prototypes in air

- Conclusions.

Requirements for high-performance TEGs

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- Use of high density NWs arrays as thermoelements in the TEGs.
- Fabrication of low resistivity NWs with n and p-type doping on the same substrate.
- Appropriate TEG design to assure high temperature gradient on the nanostructured thermocouples. Vacuum packaging technology can be also adopted to eliminate heat exchange through air and enhance the power generation.
- Fabrication of thermoelements composed by a large number of nanowires in parallel to multiply the current and use of a sufficient number of thermocouples in series to multiply the output voltage.

Nanomachining - Silicon nanowires (NWs)

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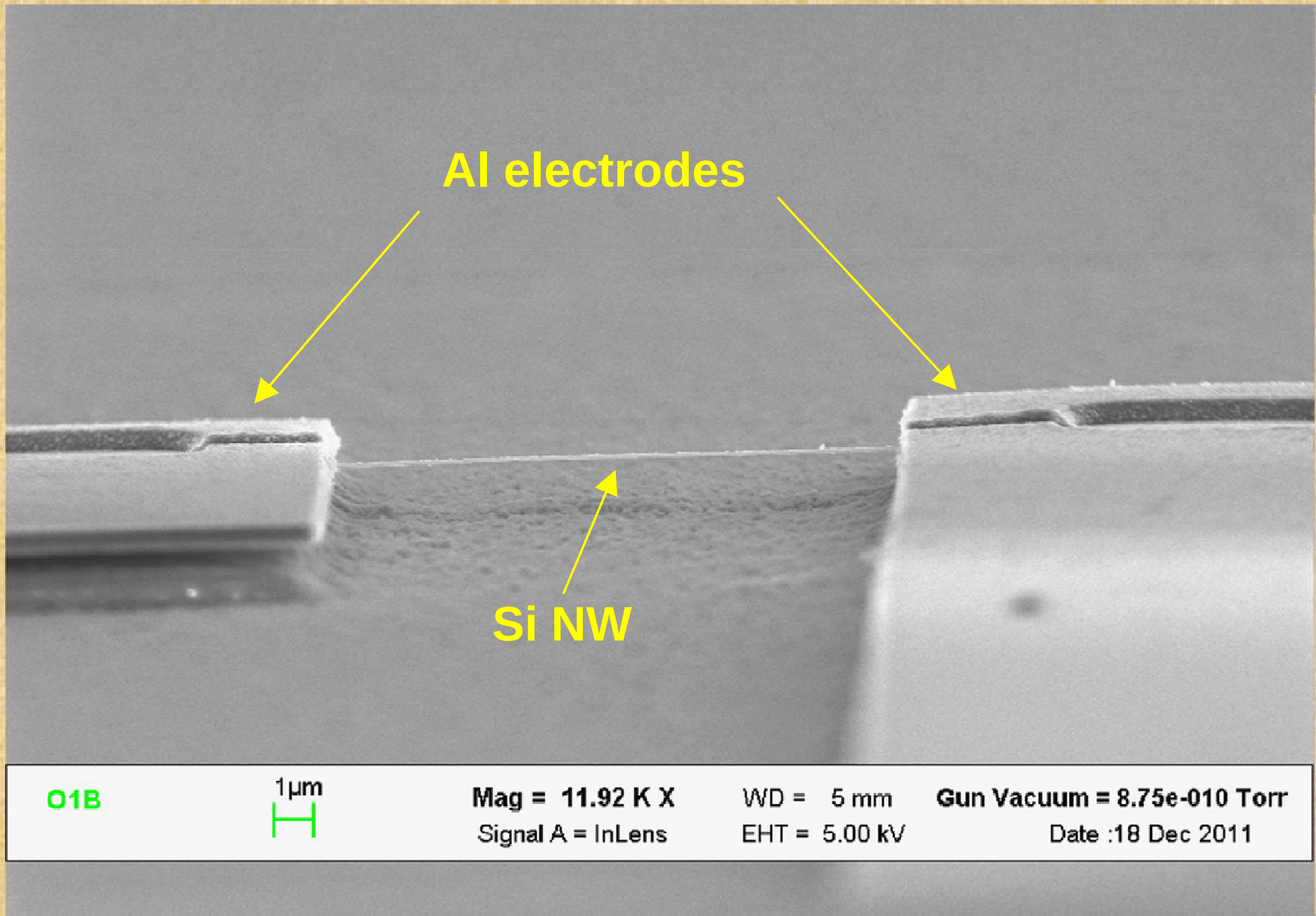
Surface-nanomachined nanowires:



Nanomachining - Silicon nanowires (NWs)

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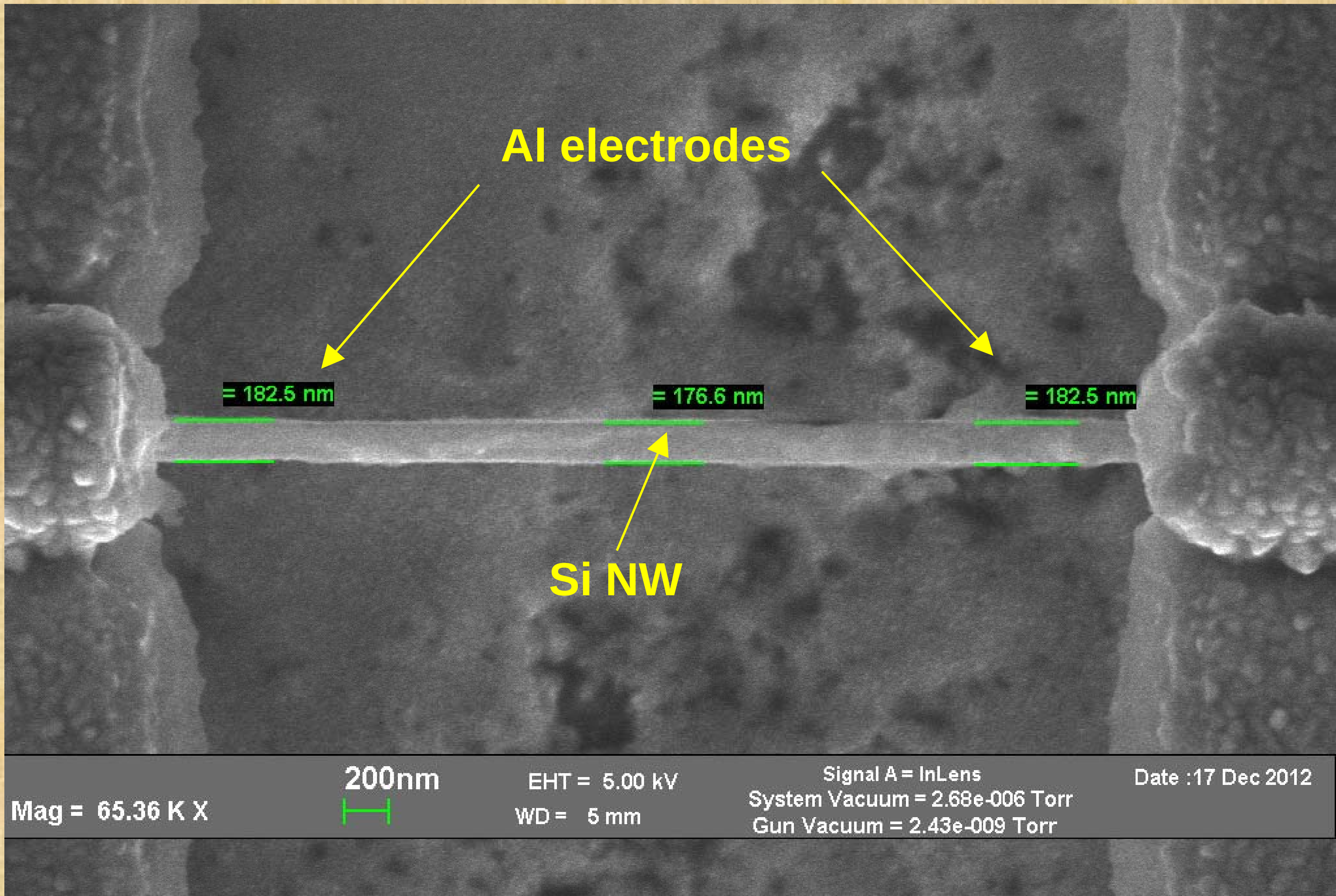
SEM characterization of NWs:



Nanomachining - Silicon nanowires (NWs)

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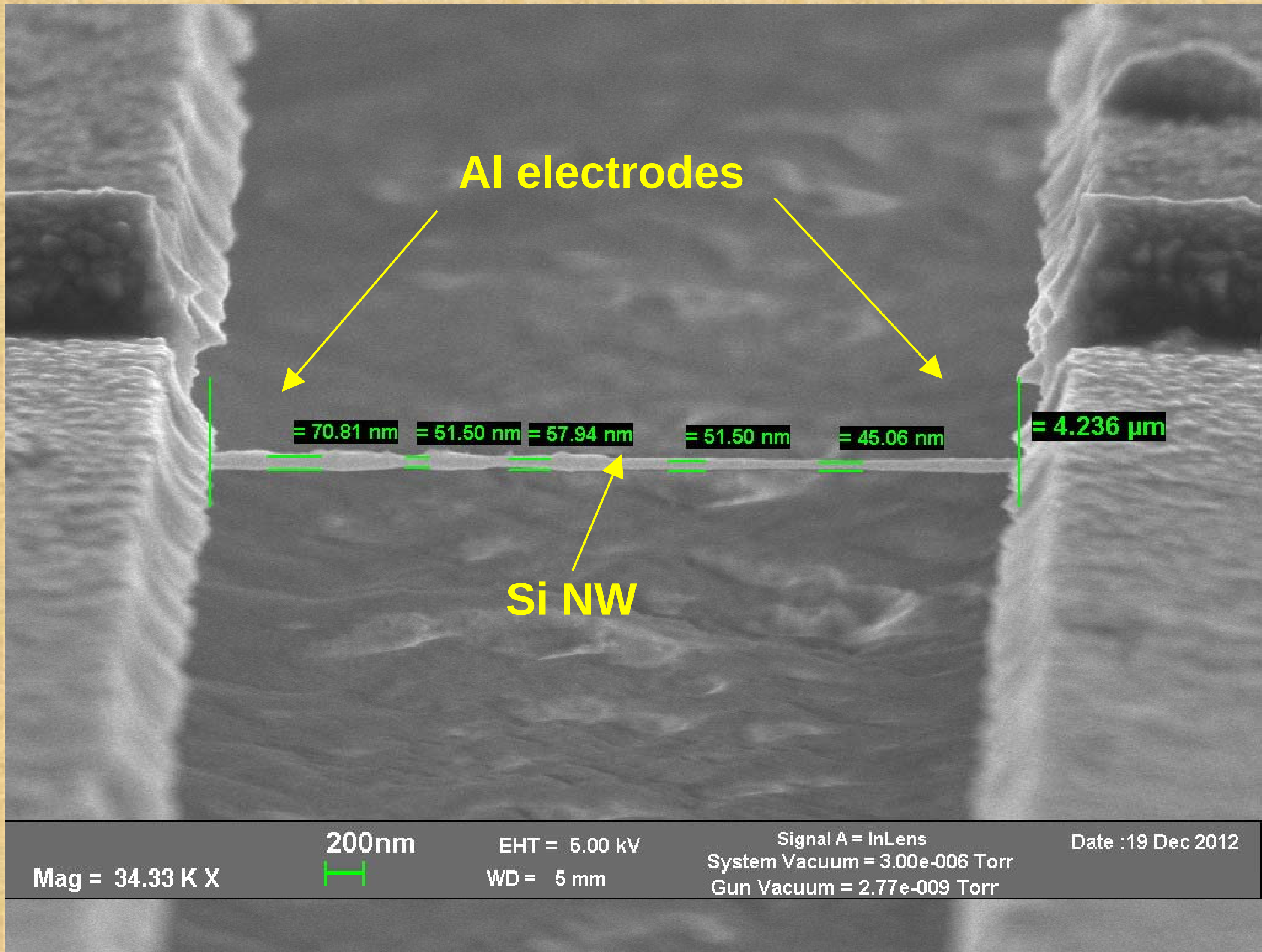
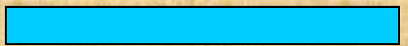
SEM characterization of NWs:



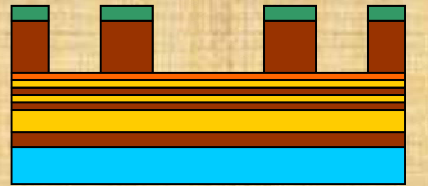
TEG - process flow (1)

1. Bulk Si

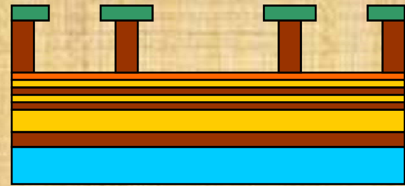


2. SiO_2/Si_3N_4/poly deposition

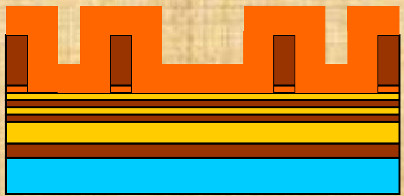
3. SiO_2 RIE



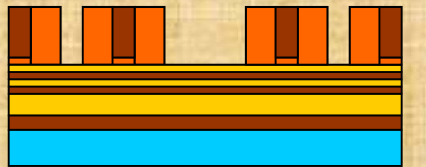
4. SiO_2 wet etching



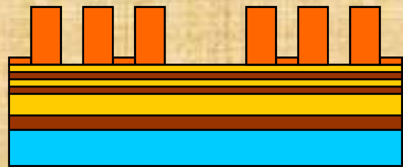
5. Poly deposition



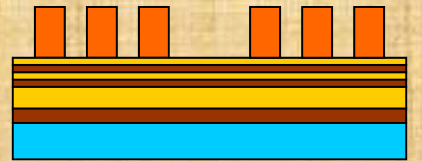
6. Poly RIE



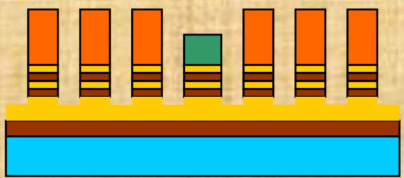
7. SiO_2 wet etching



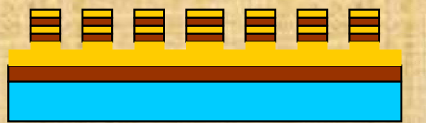
8. Poly RIE



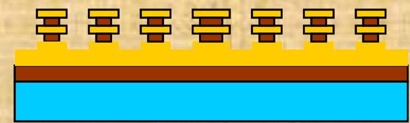
9. SiO_2/Si_3N_4 RIE



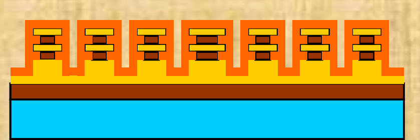
10. Poly wet etching



11. SiO_2 wet etching



12. Poly deposition



TEG based on Si NWs – fabrication

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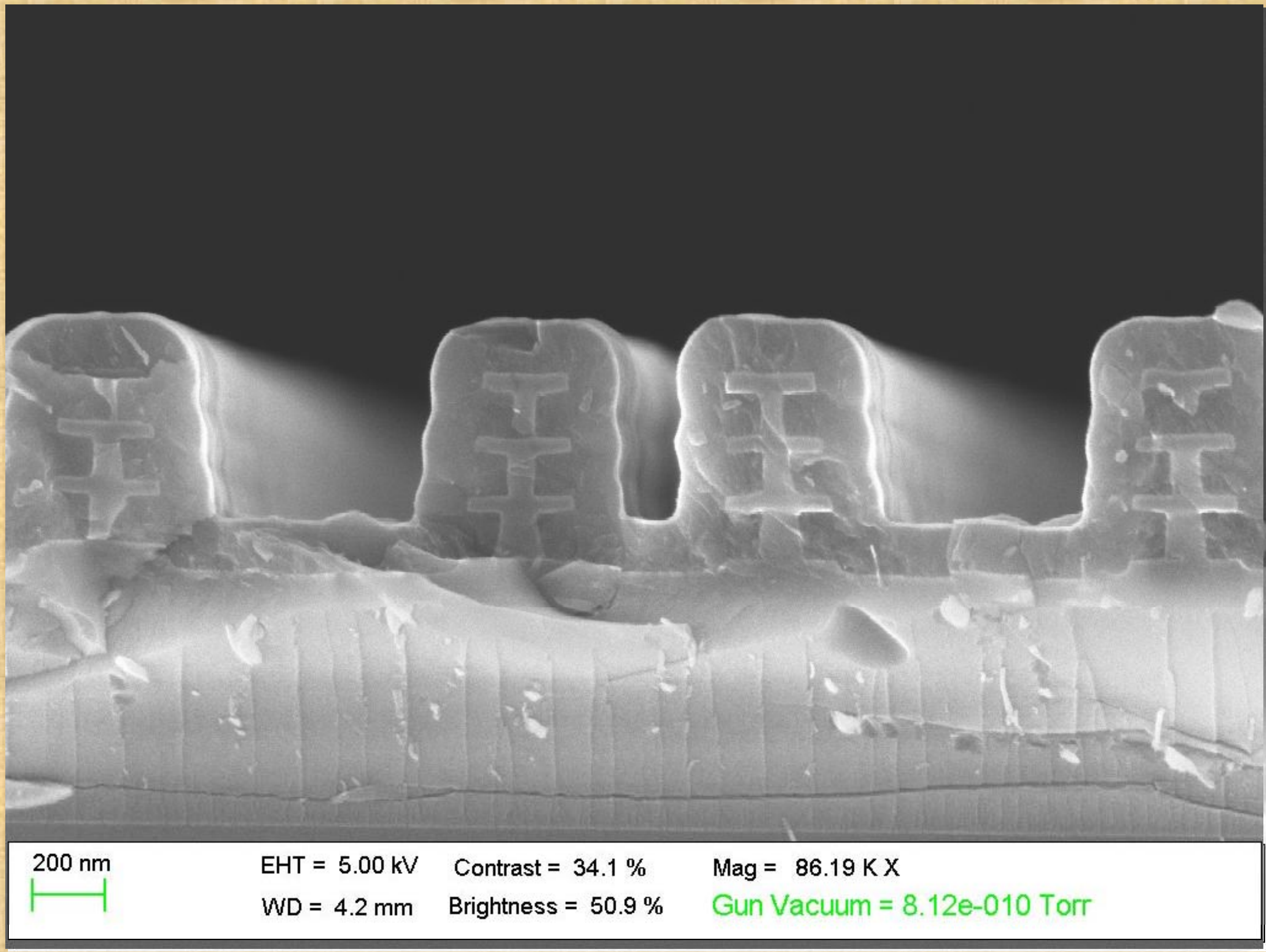

TEG based on Si NWs – fabrication

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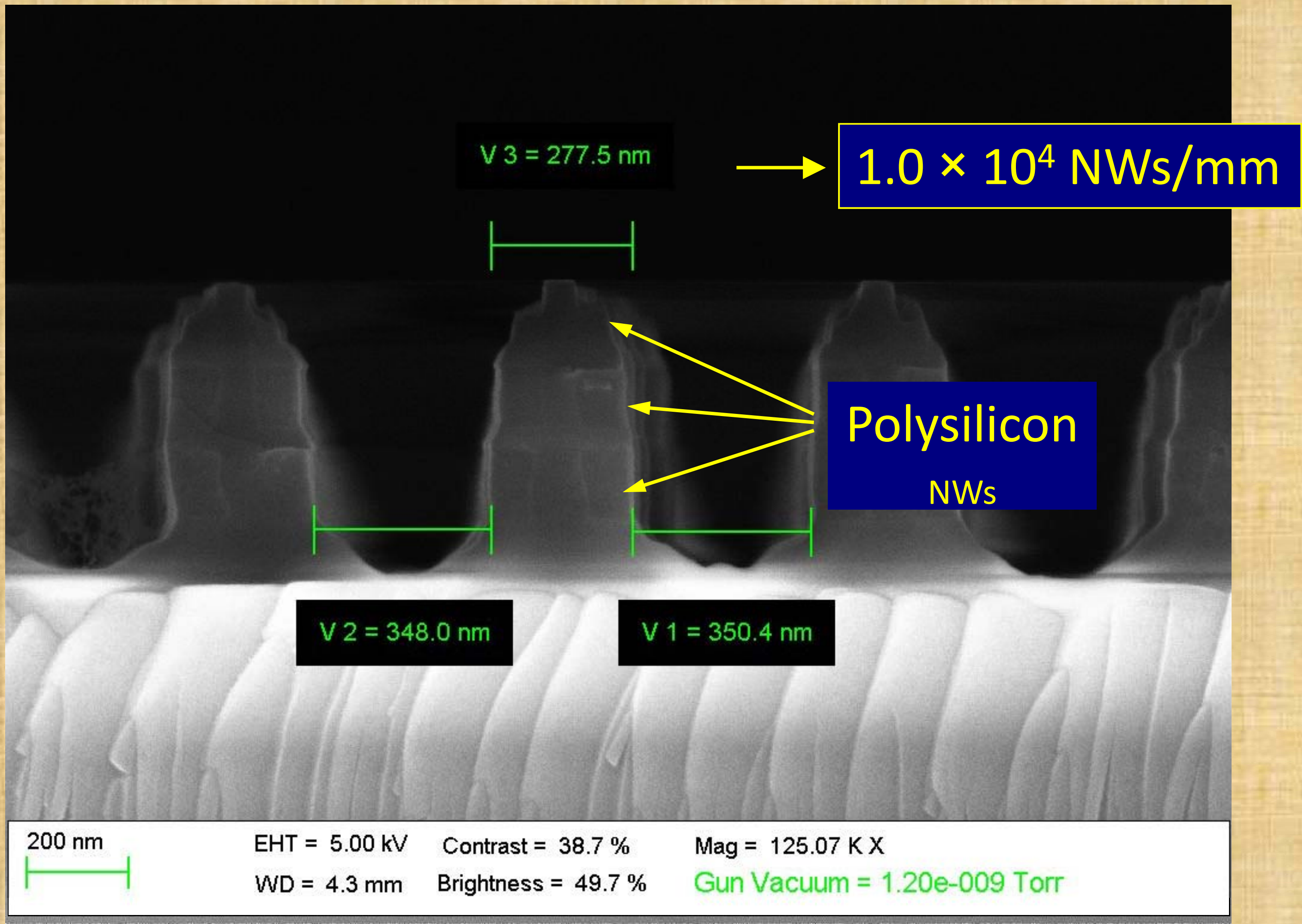

TEG - process flow (2)

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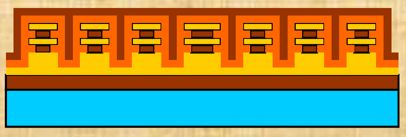
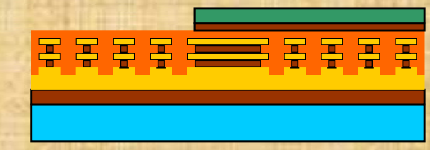
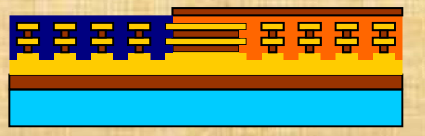
13. SiO_2 deposition



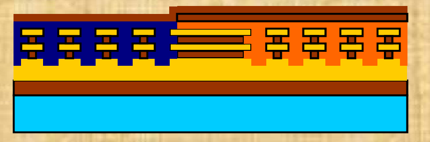
14. SiO_2 wet etching



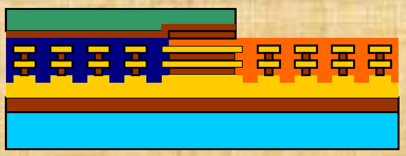
15. P-type doping



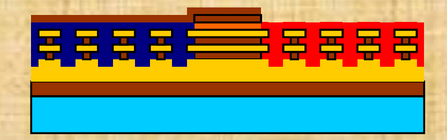
16. SiO_2 deposition



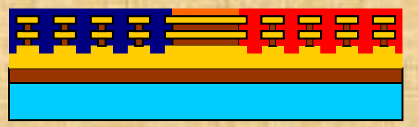
17. SiO_2 wet etching



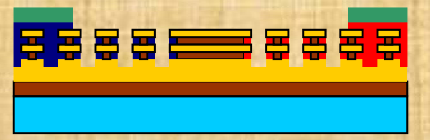
18. N-type doping



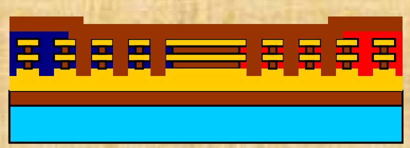
19. SiO_2 wet etching



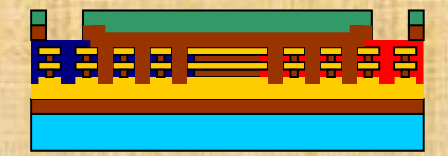
20. Poly RIE



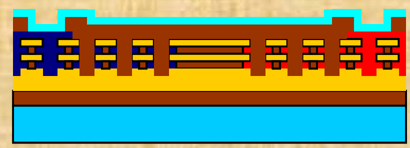
21. SiO_2 deposition



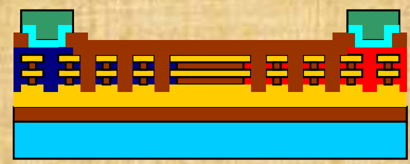
22. SiO_2 wet etching



23. Al/Si deposition



24. Al/Si etching



Thermoelectric generator based on Si NWs

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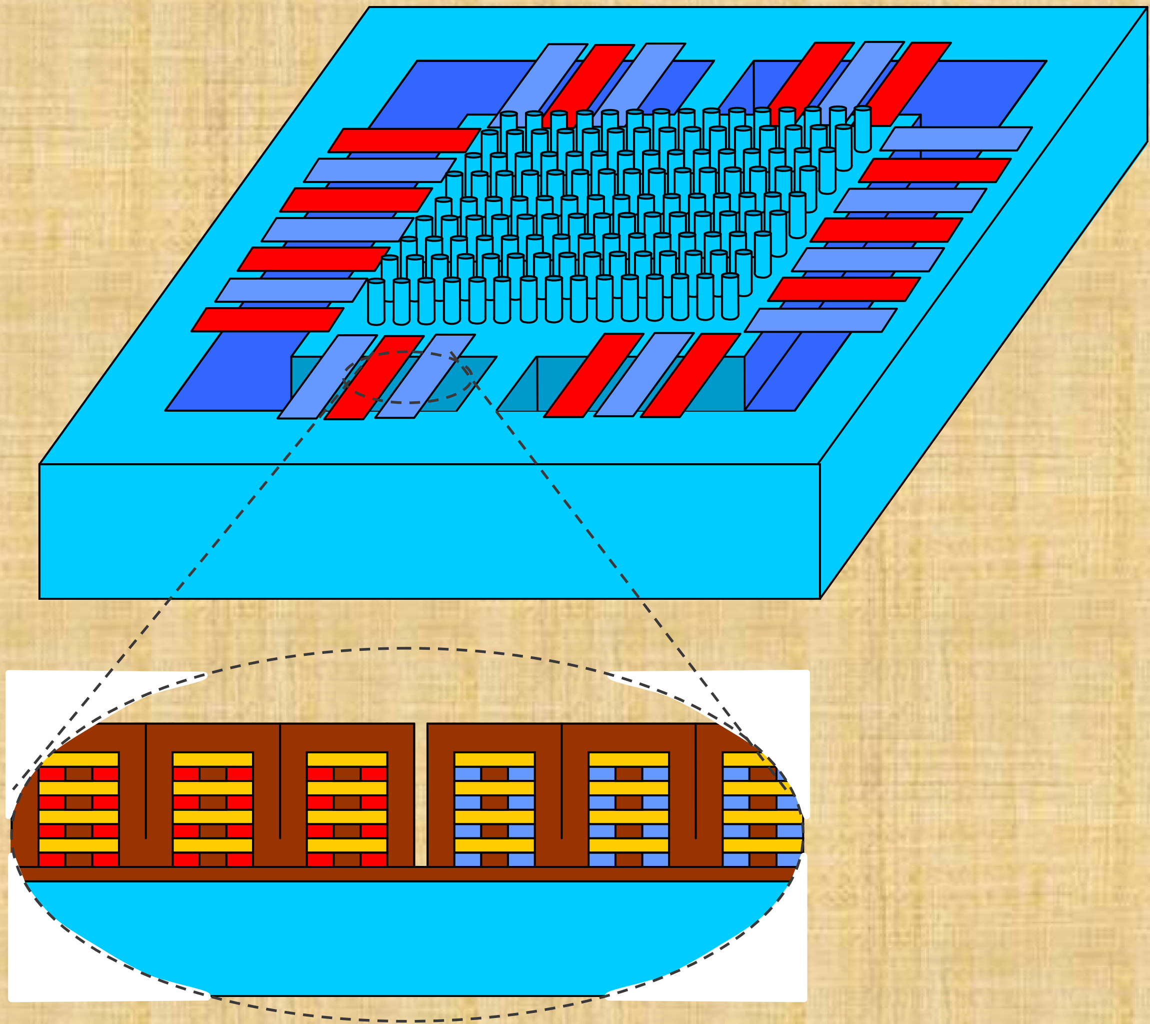

Thermoelectric generator based on Si NWs

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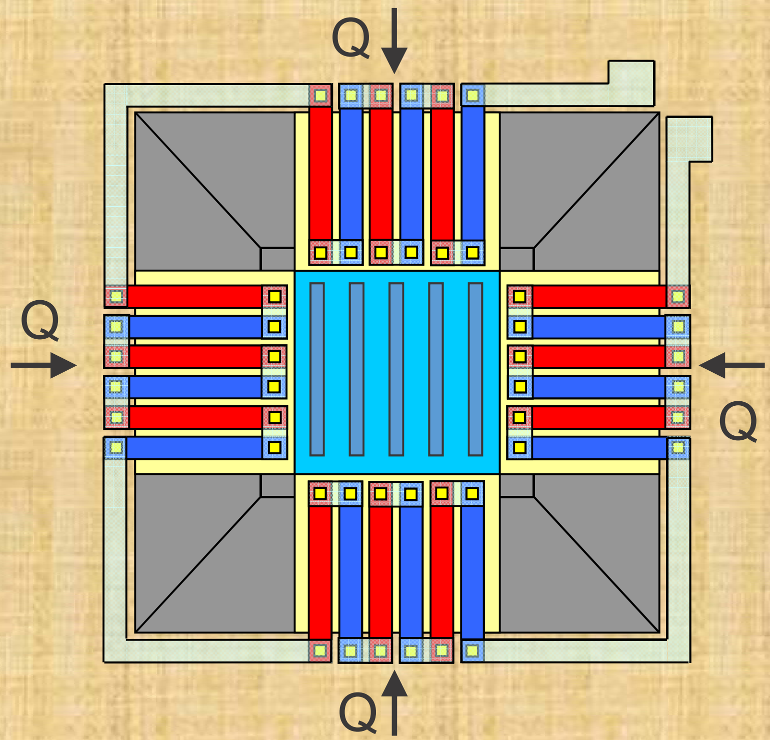

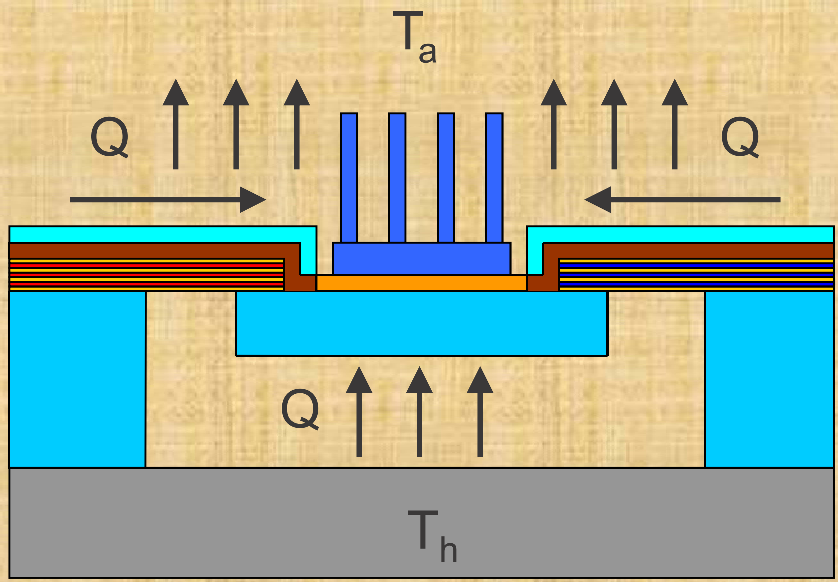

IV measurements on NWs

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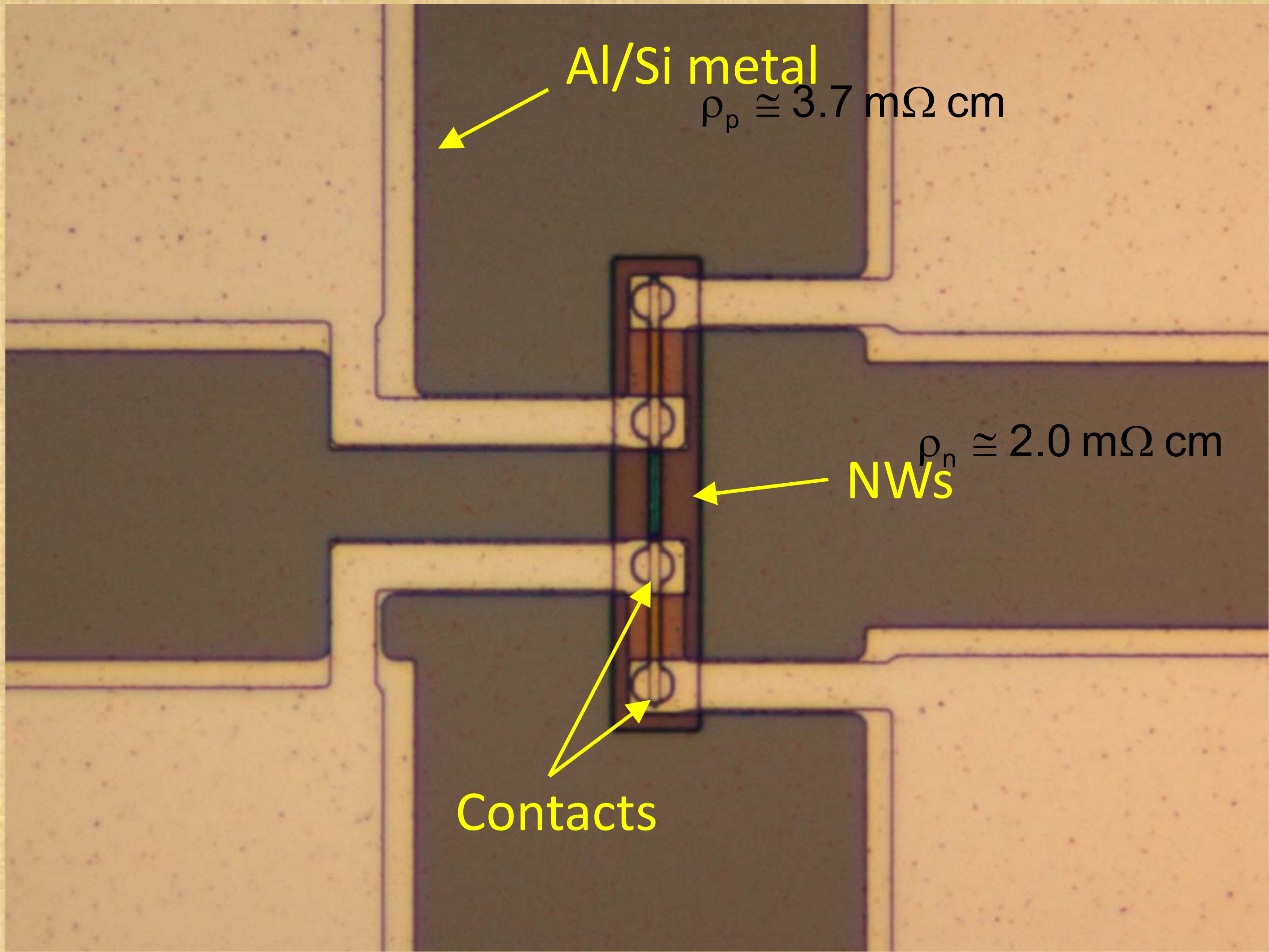
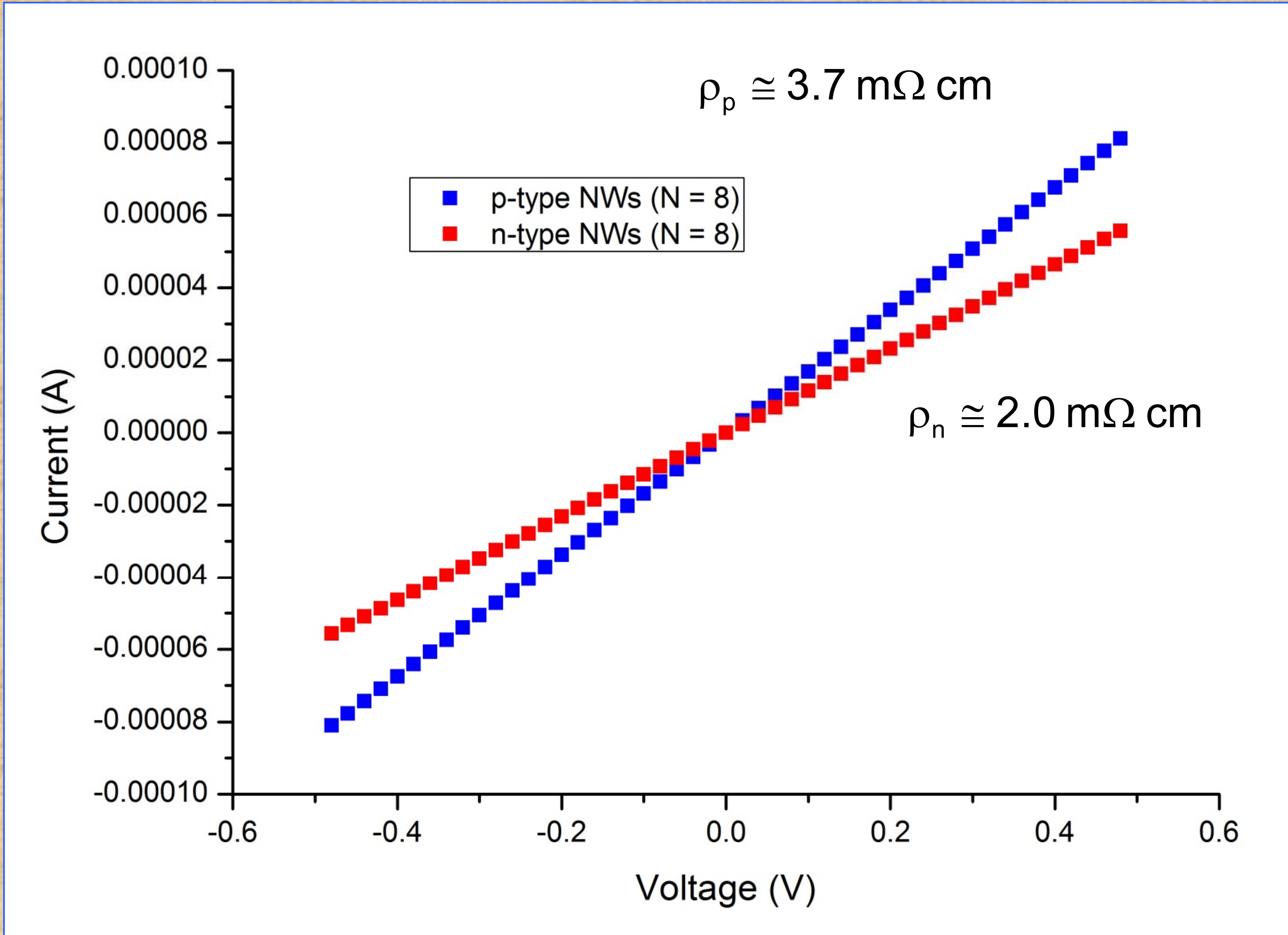


IV measurements on NWs

IMM Bologna



IV measurements on NWs

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By combining thermal simulation and electrical measurements the thermal conductivity has been also estimated for the fabricated geometry:

Sample	Doping	Resistivity [mΩ·cm]	Length [µm]	Thickness [nm]	Width [nm]	Conductivity [W/mK]
A	B	5.1	4.8	180	70	2.3
B	B	5	4.8	173	70	2.1
C	B	6.2	4.8	166	62	1.8
D	P	1	6.6	172	70	4.5
E	P	1	6.6	172	67	4
F	P	1.7	6.6	140	30	3.4

$k_{\text{p-type}} \approx 2$ W/mK

$k_{\text{n-type}} \approx 4$ W/mK

Thermal conductivity of polysilicon nanowires used as thermocouple elements

Seebeck measurements on NWs

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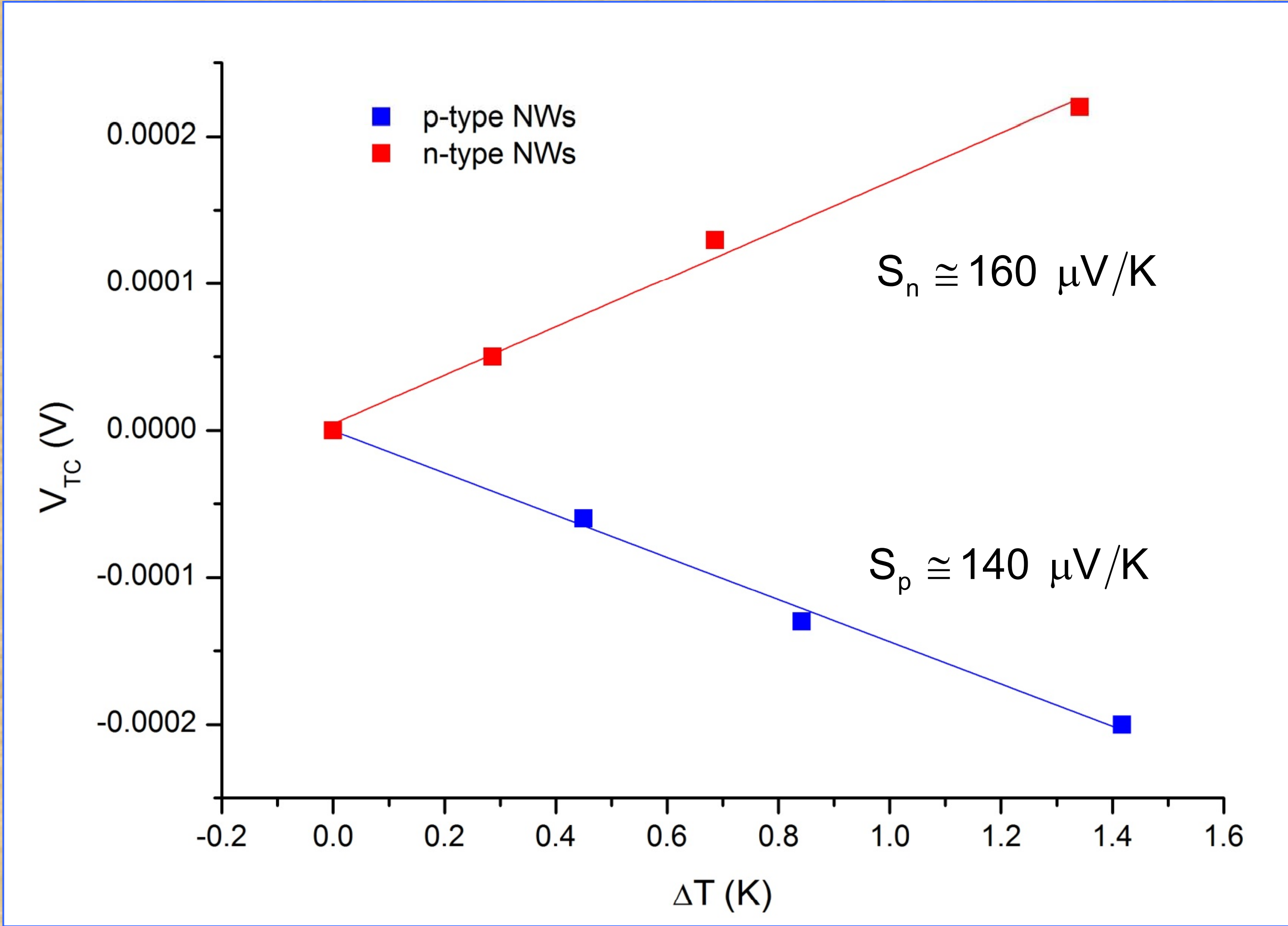

TEG based on Si NWs – fabrication

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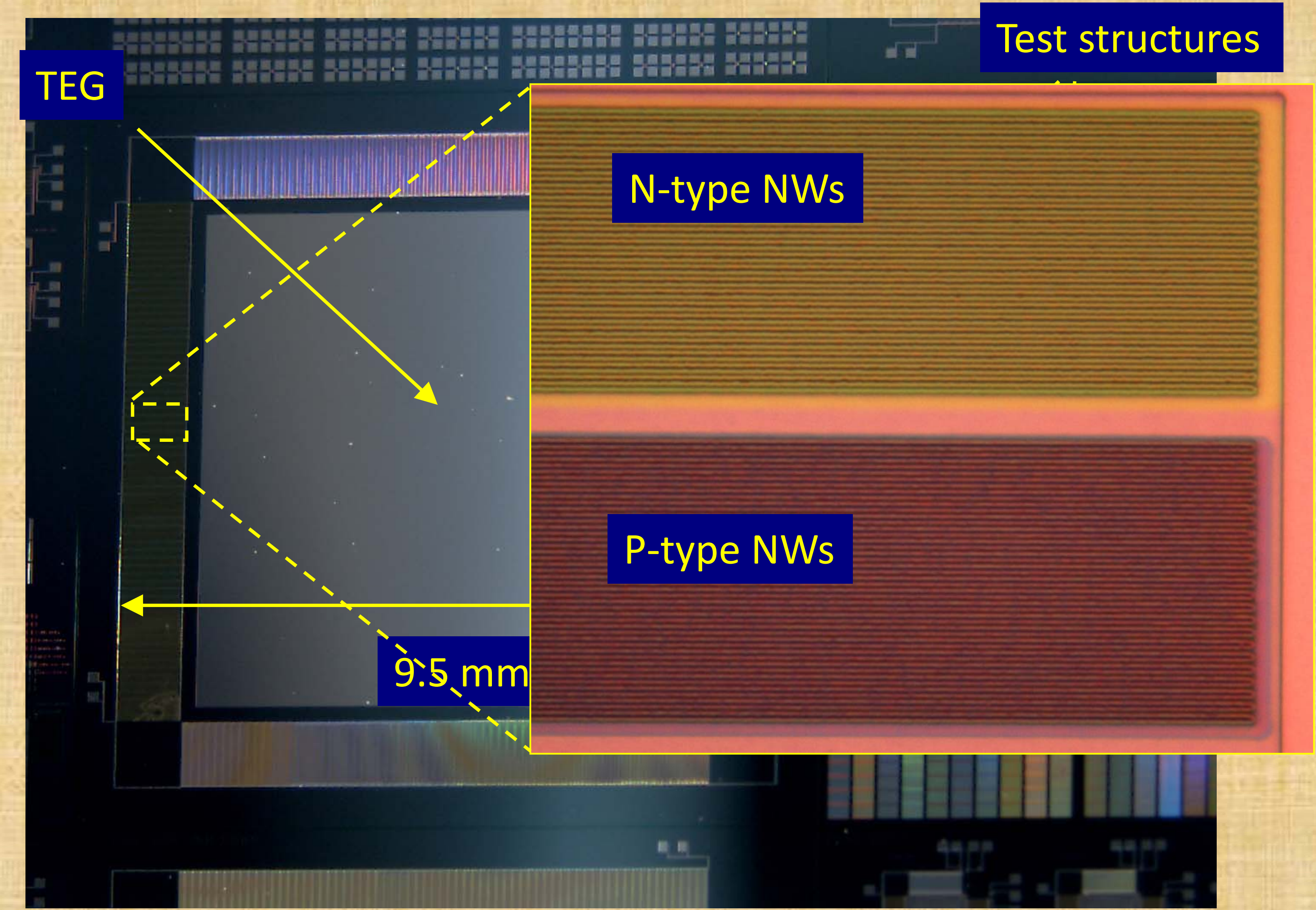

TEG based on Si NWs – testing

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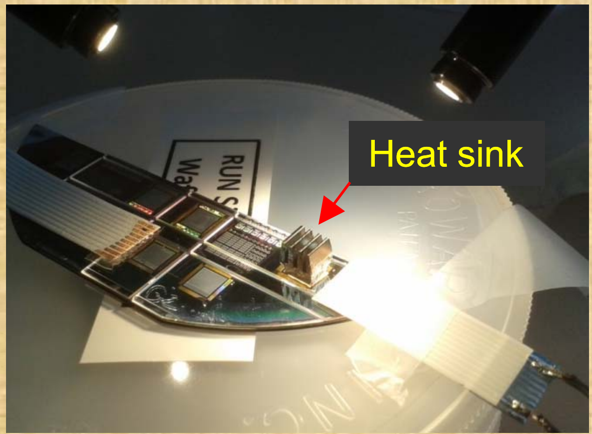
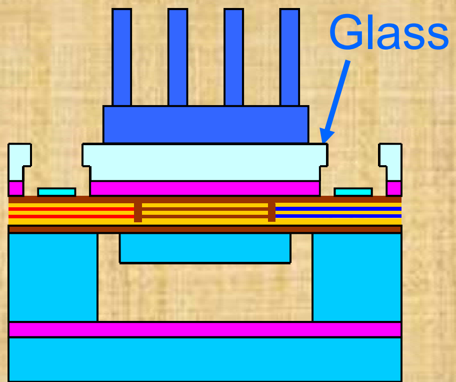
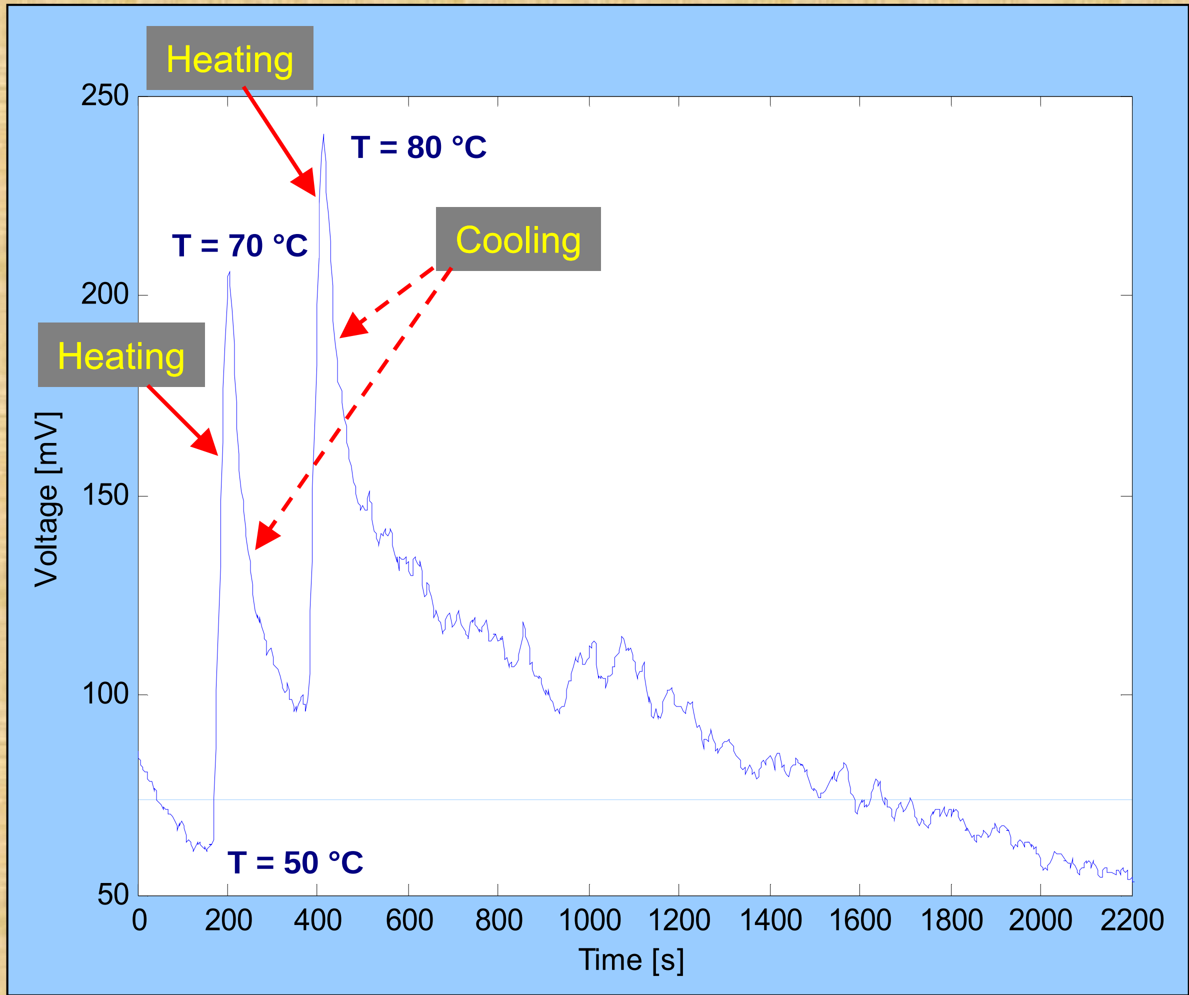
TEG prototype





Test result on hotplate



Testing of TEGs

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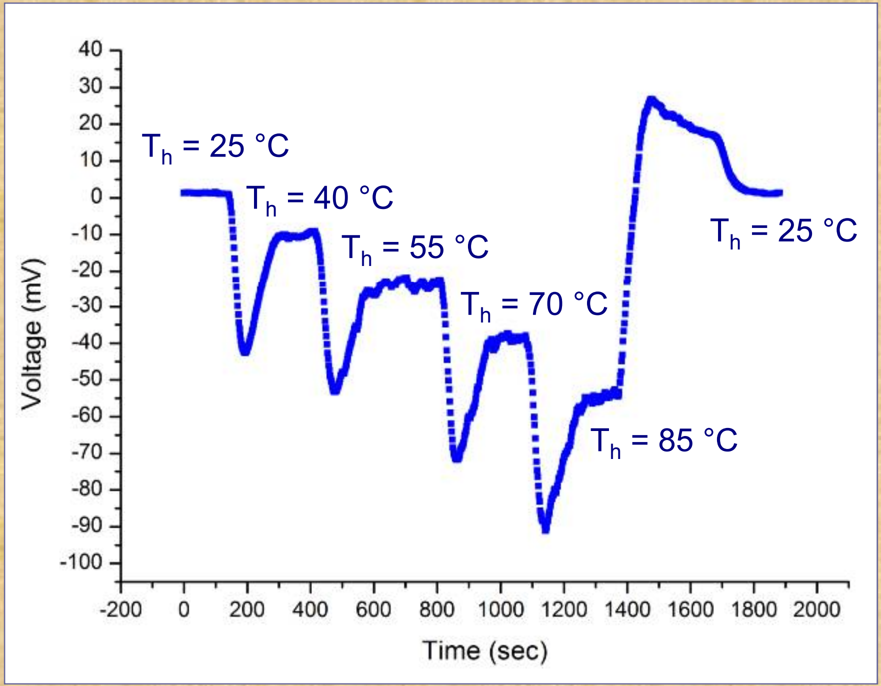
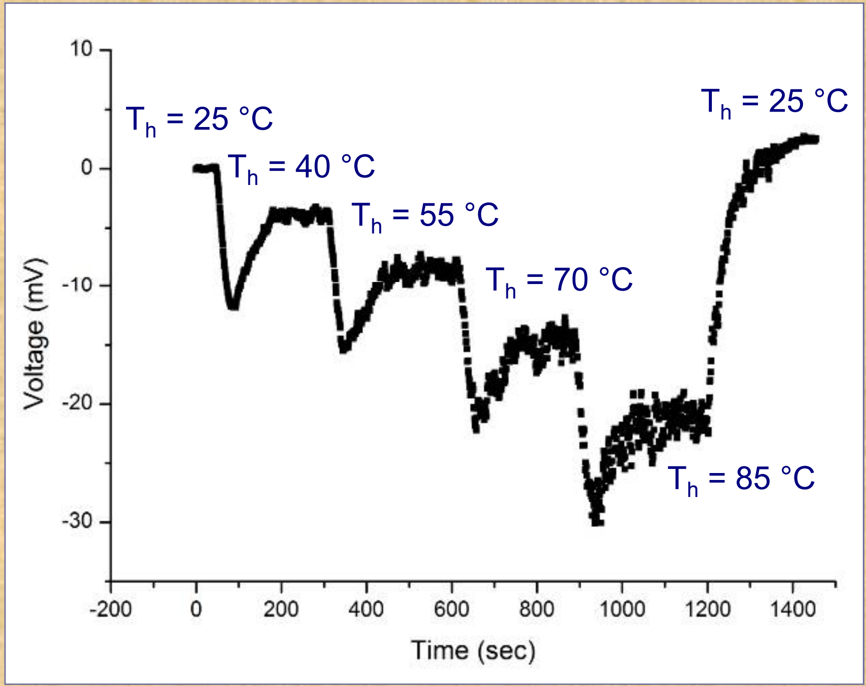
TEG with heat sink



TEG without heat sink



TEGs performance on first-generation device was estimated to be of roughly 50 nW output power for operation at 200 °C.

However the power generation was basically limited from the thermal conductance of thick glass used to make the structure robust enough for the radiator application. Considerable performance improvements are expected using thinner glass cap wafer.

Second generation of lateral TEGs in air

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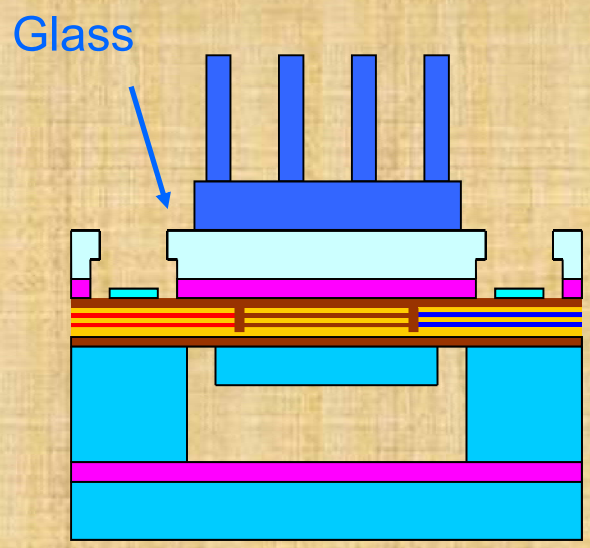
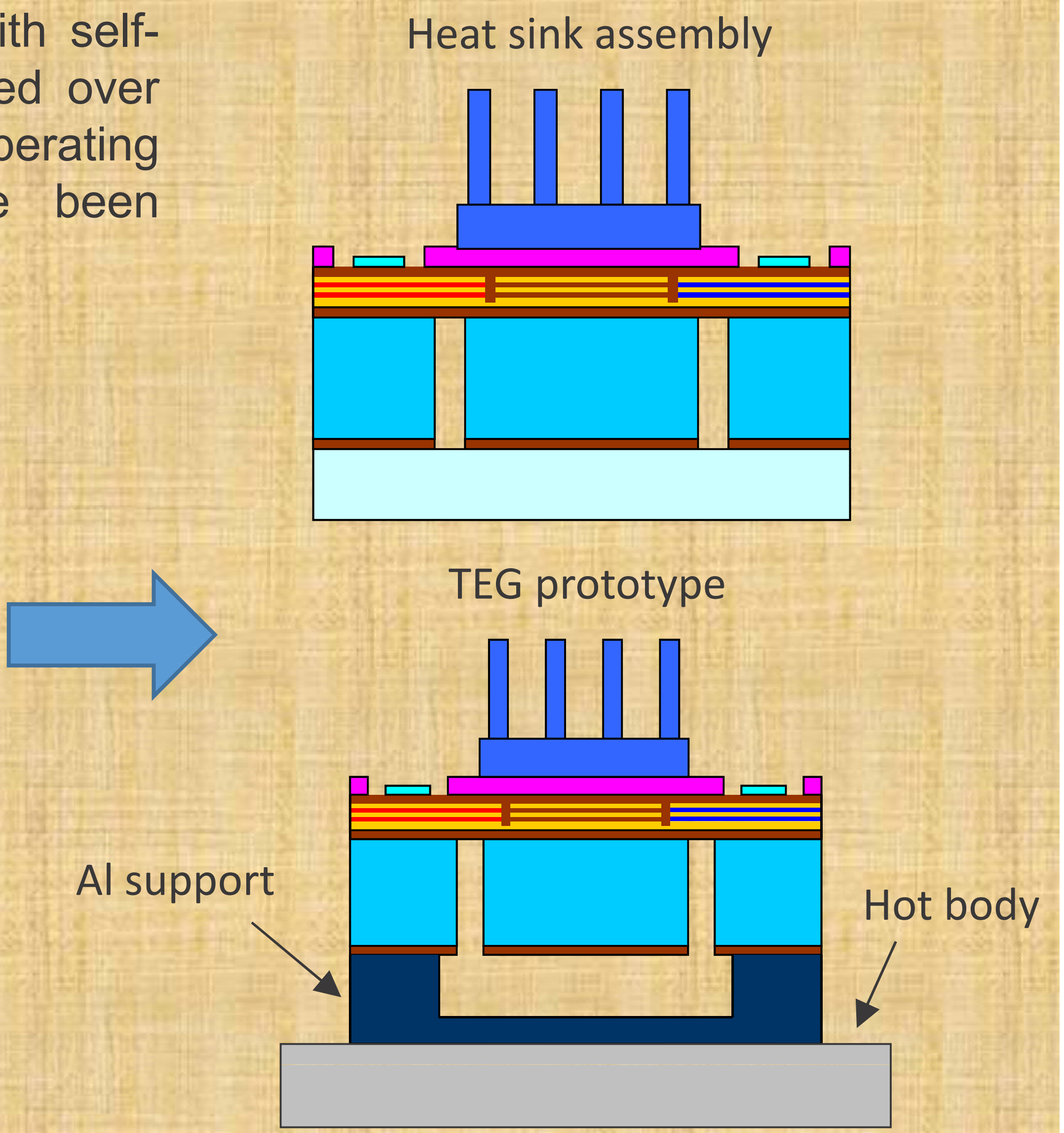
New prototypes of lateral TEGs with self-standing bulk Si masses suspended over SiO_2/Si_3N_4/SU-8, suitable for operating without vacuum packaging have been manufactured.



TEGs with vacuum technology



Second generation of lateral TEGs in air - backside micromachining

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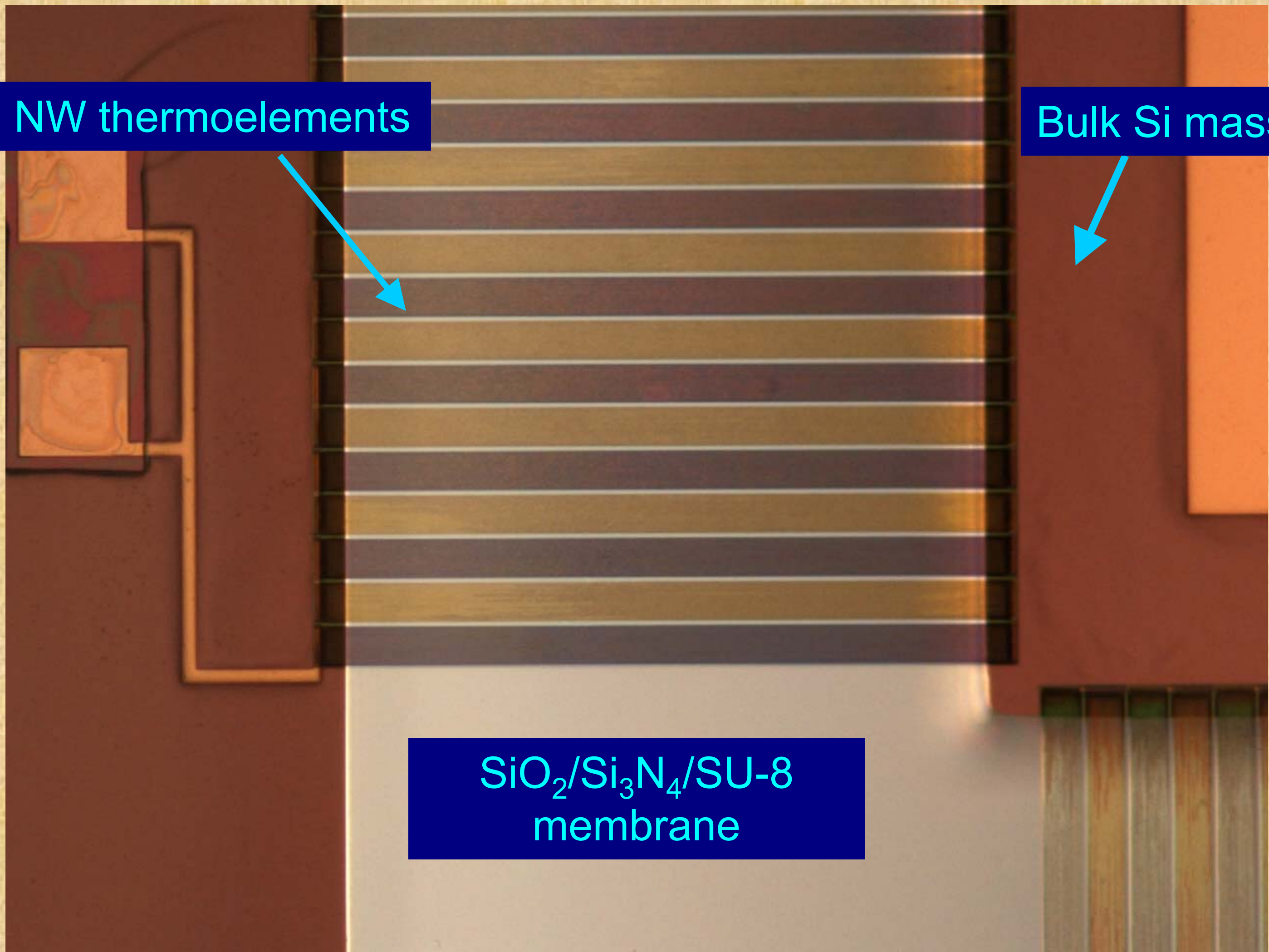

Testing – Functional testing of the TEGs

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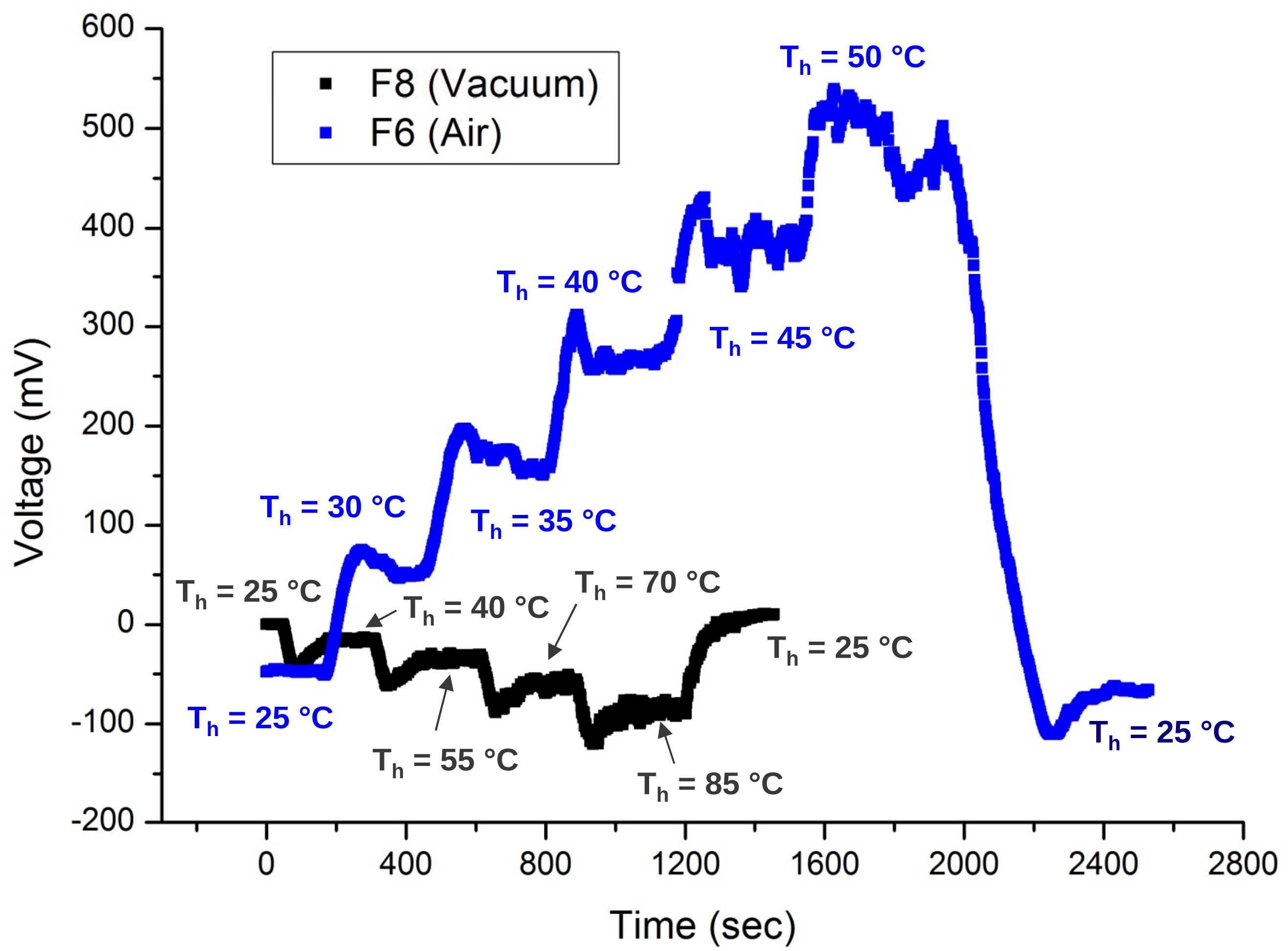
Comparison of F6 (8 mm) in air and F8 (8 mm) in vacuum, both without radiator:



Gain in output power of a factor around 100 with respect to the first generation devices.

Conclusion

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- NW arrays with linear density of 1.0×10^4/mm have been obtained.

- On the high-density NWs, electrical resistivity values around 2.0 mΩ cm with n-type doping and 4.0 mΩ cm with p-type doping have been achieved.

- The measured Seebeck coefficient was around 150 μV/K for both doping types.

- The measured thermal conductivity was around 2 W/mK for p-type doping (Boron) and 4 W/mK for n-type doping (Phosphorous).

- The new prototypes without glass cap have been tested yielding a gain in output power of a factor around 100 with respect to the first generation devices. TEGs performance is expected to be of roughly 4 μW/cm^2 output power for operation at 200 °C with heat sink, sufficient for powering a sensor node.

- Optimization of the performance for the TEGs designed with vacuum technology is possible by thinning the glass cap wafer.

Thank you for your attention!

L. Belsito, F. Mancarella, A. Roncaglia

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Institute for Microelectronics and Microsystems (IMM), CNR (Italy)

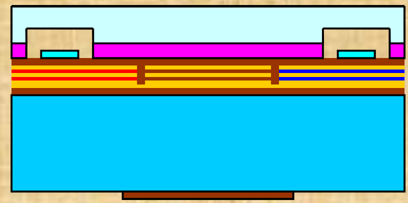
SEVENTH FRAMEWORK PROGRAMME

TEG - process flow (3)

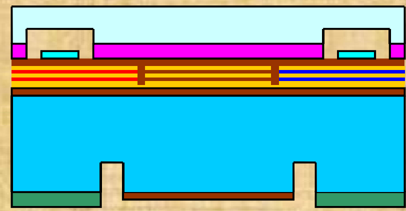
25. Wafer with NWs

26. SiO_2/Si_3N_4 RIE

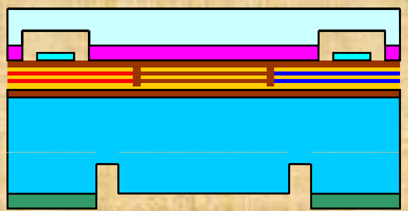
27. Wafer bonding



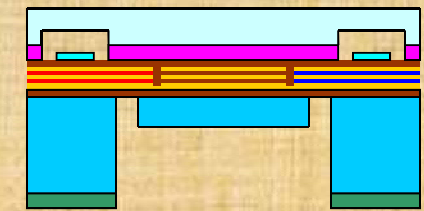
28. Si DRIE



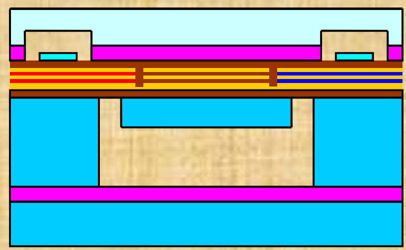
29. SiO_2 etching



30. Si DRIE



31. Wafer bonding



32. Glass dicing