WP2
Thermoelectric Harvesting

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SiNERGY

Outline

Redundant TEG strategies:

- bottom-up, by VLS
- top-down by non-critical lithography

Modeling set up to optimize wire lengths upon heat source characteristics

All technologies are IC-compatible to support integration in the final prototype

Strategy and device layouts

Goal: Obtain all-silicon thermoelectric micronanogenerators by means of the integration of silicon based NW arrays (as thermoelectric material) into a Si micromachined structure able to exploit a waste heat source to develop an internal thermal contrast between two isolated silicon parts.

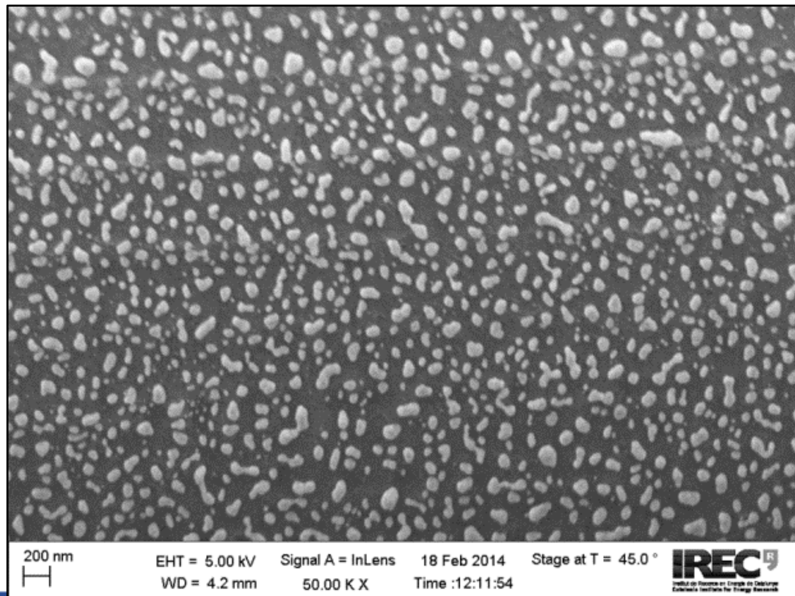
Bottom-up strategy

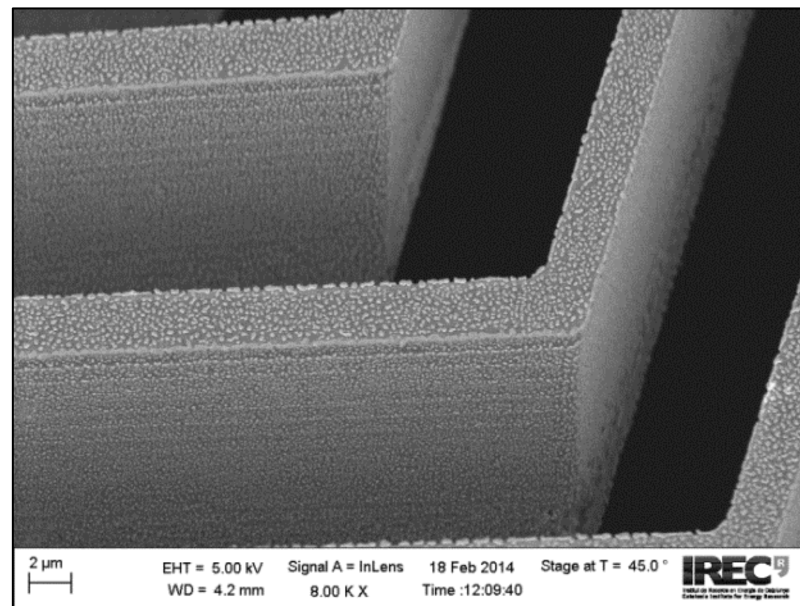
NWs will be grown with a VLS-CVD method that allows the in-situ integration of large density arrays of NWs within a 3D structure without specific nanolithography techniques.

Microemulsion Galvanic Displacement

To seed the surface with gold nanoparticles, devices are

1. **dipped in HF** in order to remove native oxide from trenches
2. **dipped in microemusions** during a controlled dipping time. Gold NPs are formed
3. **annealed** to remove the remaining surfactant

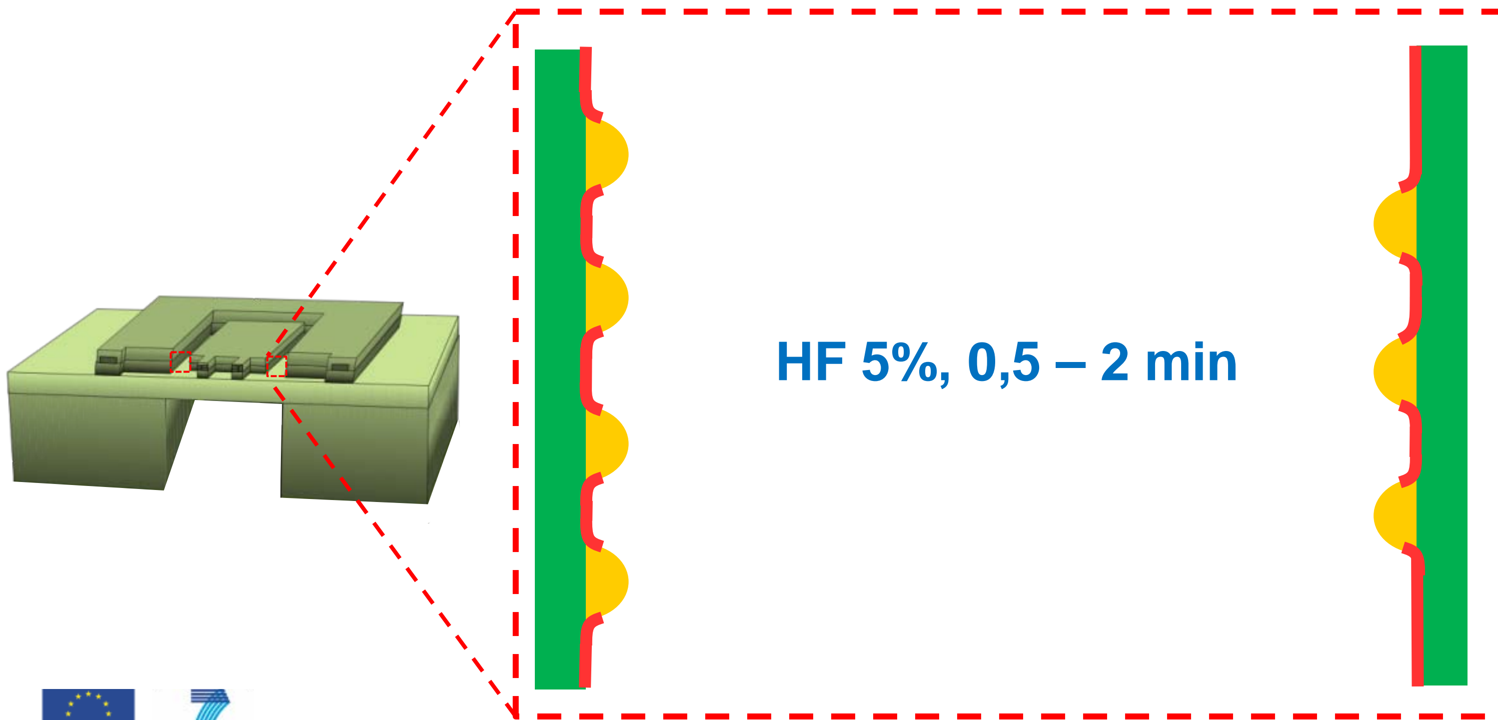




Gao et al, J. Am. Chem. Soc. 127, 4574 (2005)

CVD-VLS growth of NWs

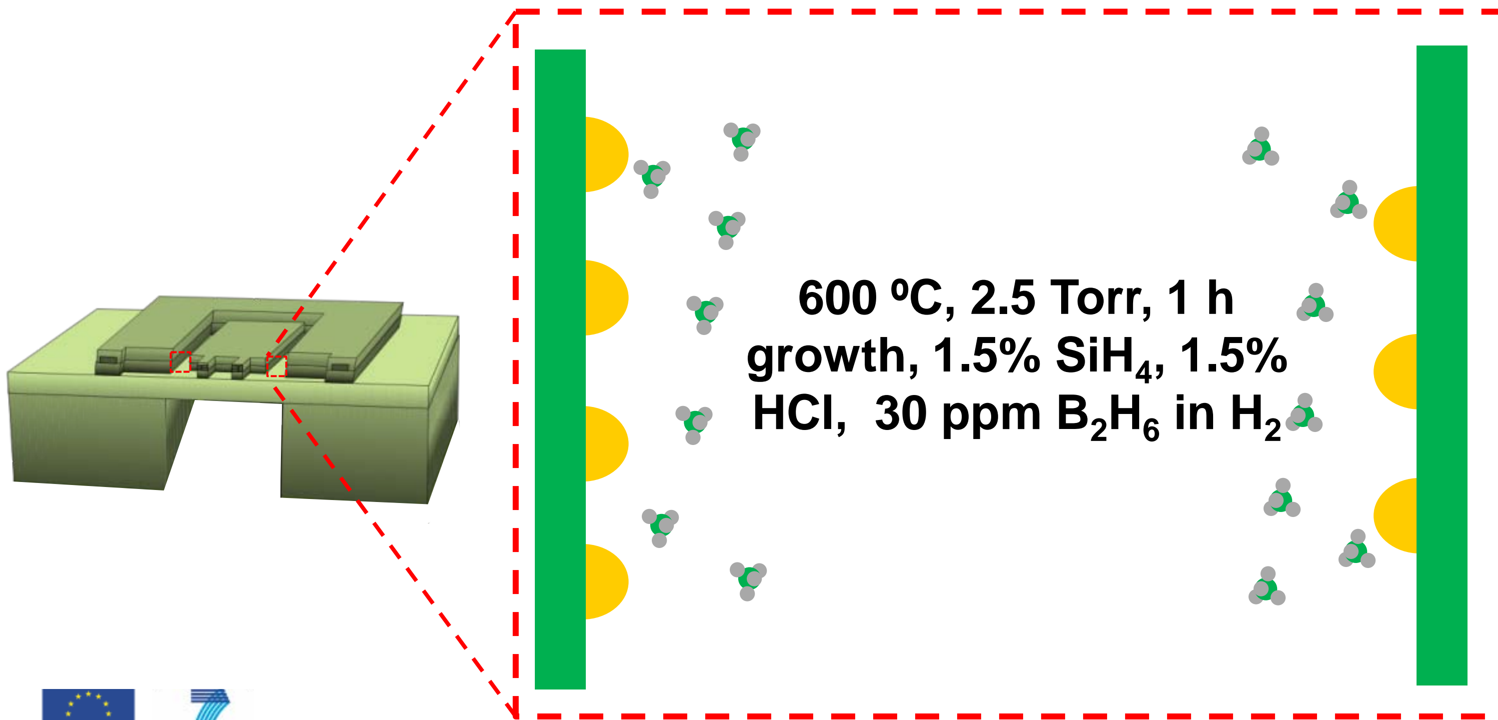
1 – Devices are dipped in **HF** in order to remove thermal oxide formed during calcination



CVD-VLS growth of NWs

1 – Devices are dipped in **HF** in order to remove thermal oxide formed during calcination

2 – Devices are loaded into **CVD and exposed to silane**. Silicon nanowires are grown by VLS synthesis



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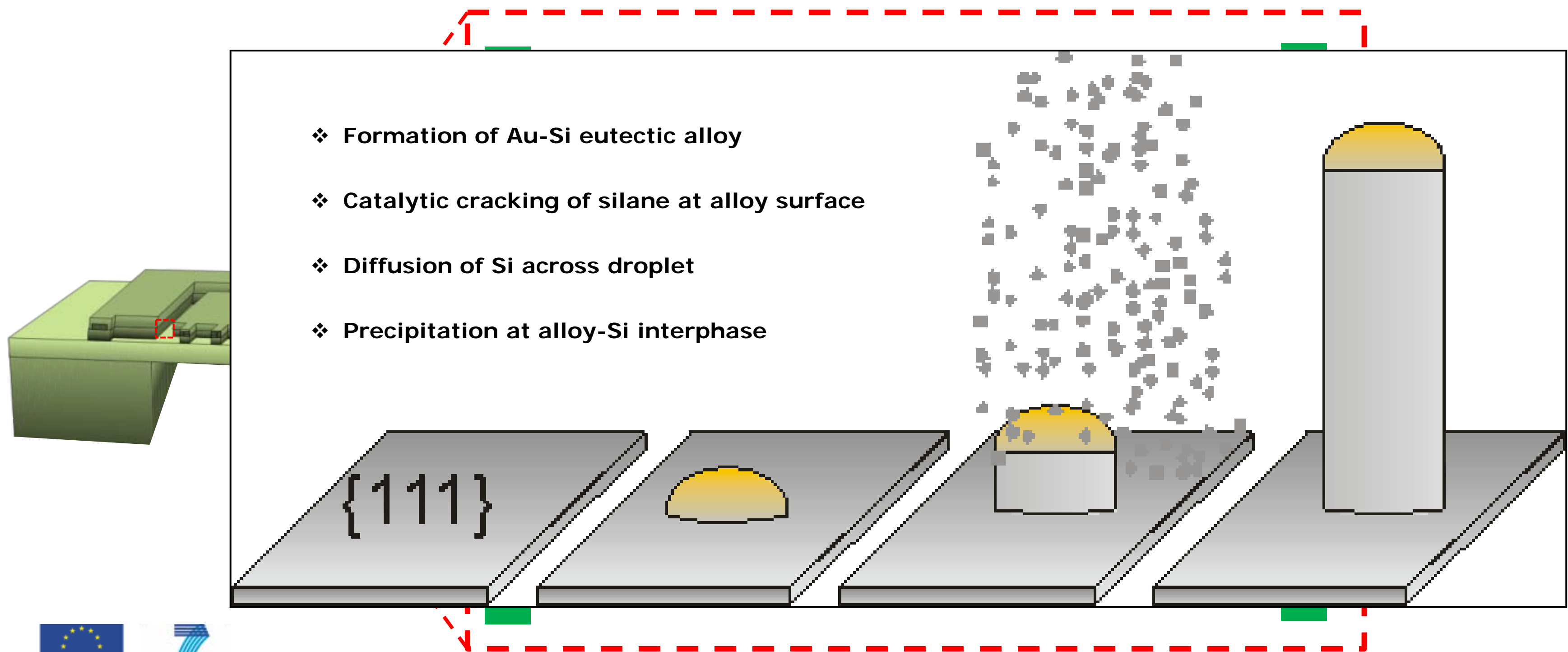

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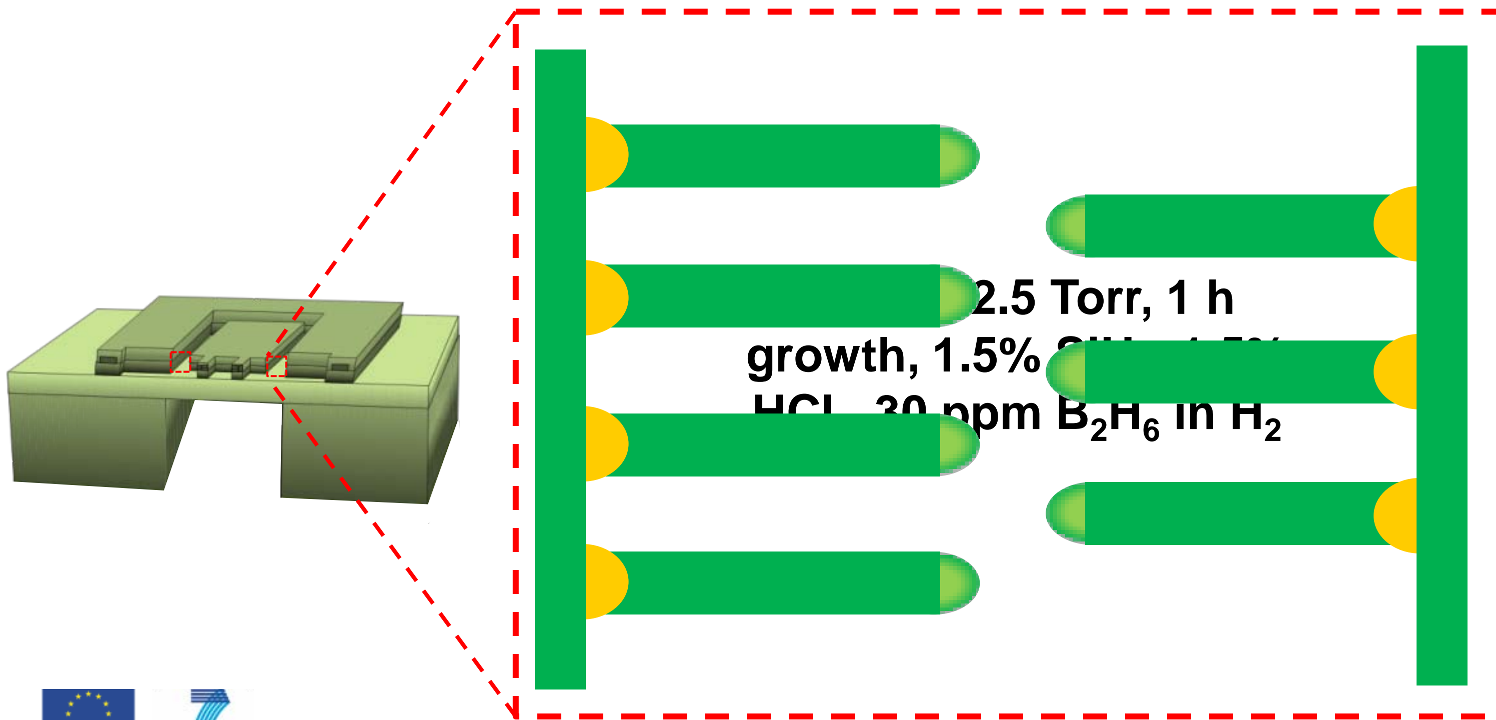

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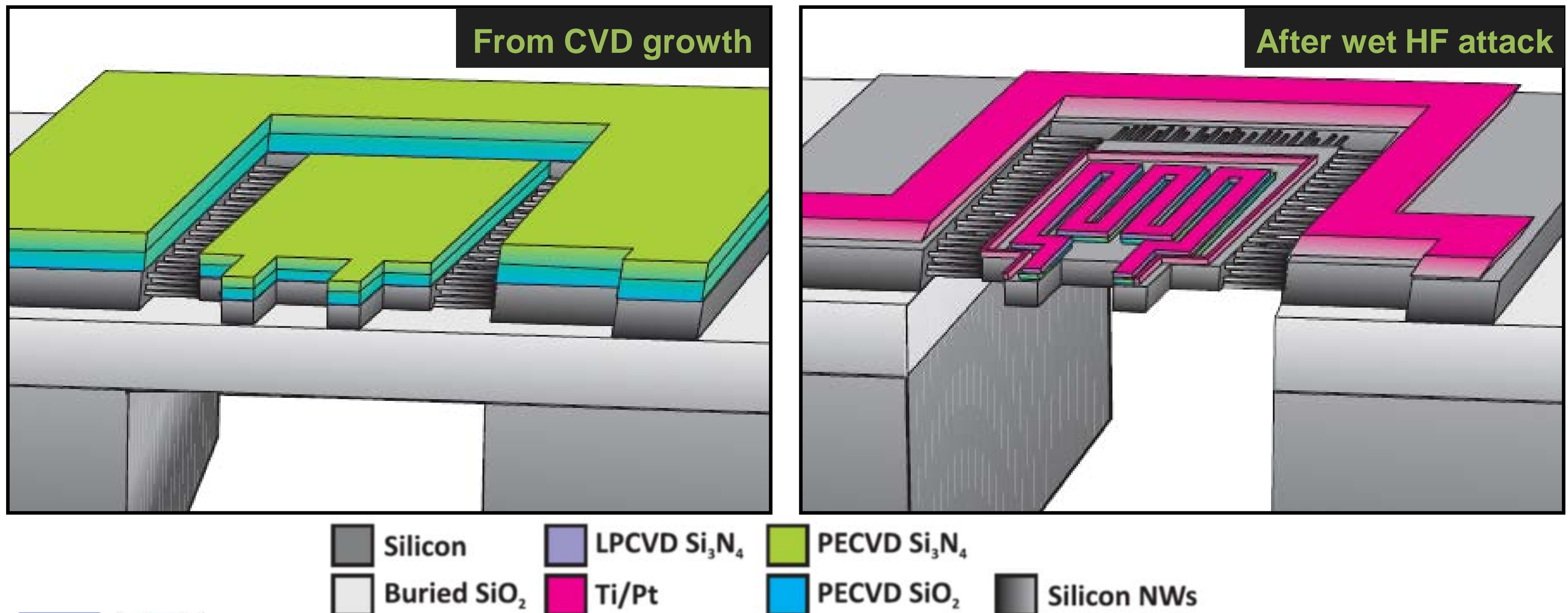
Membrane removal in HF

After growing Si NWs in a µTEG device a wet attack in HF must be performed in order to remove membrane and passivation silicon oxide – which covers contacts.



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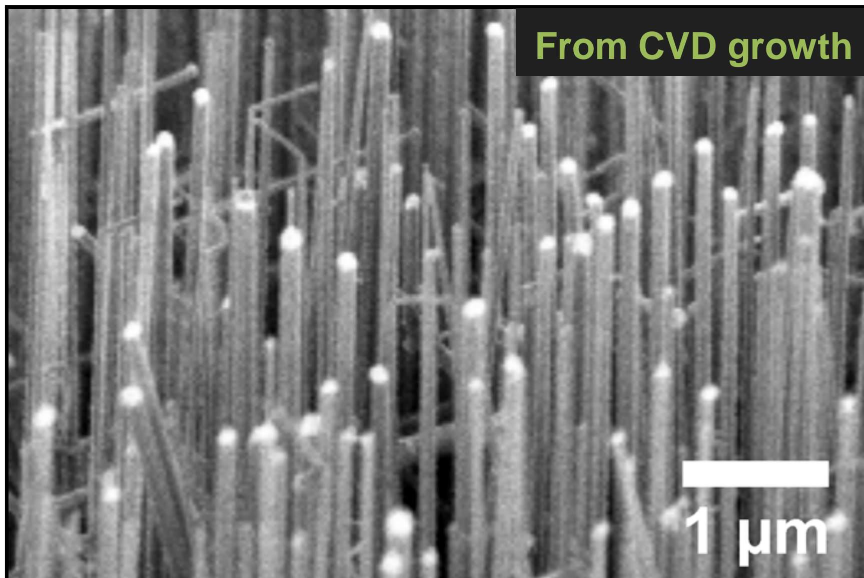

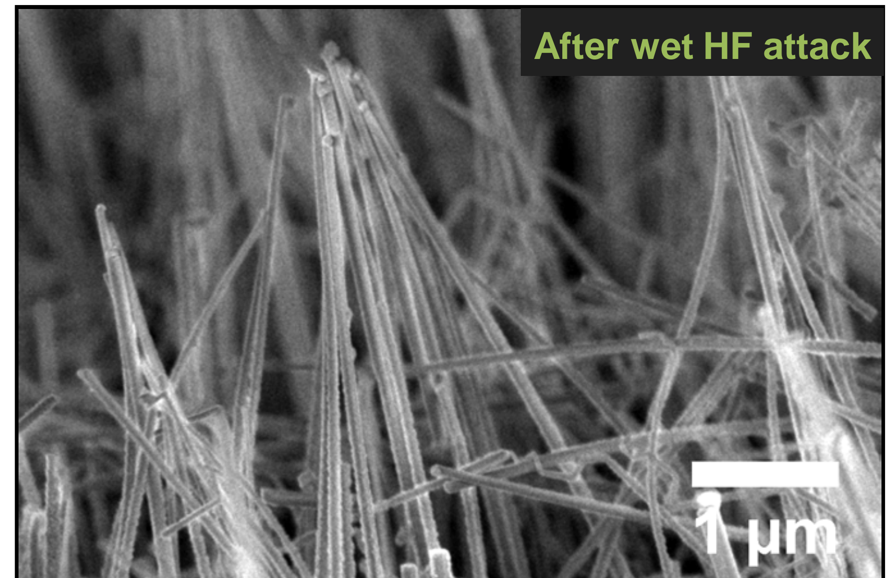

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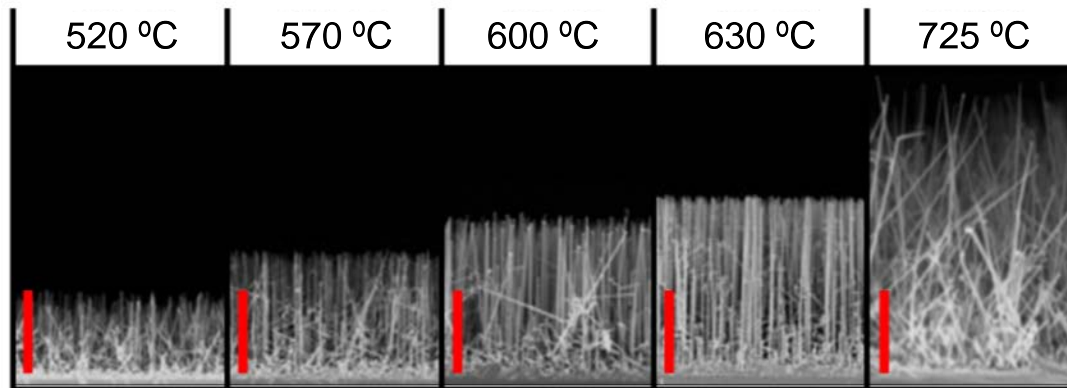
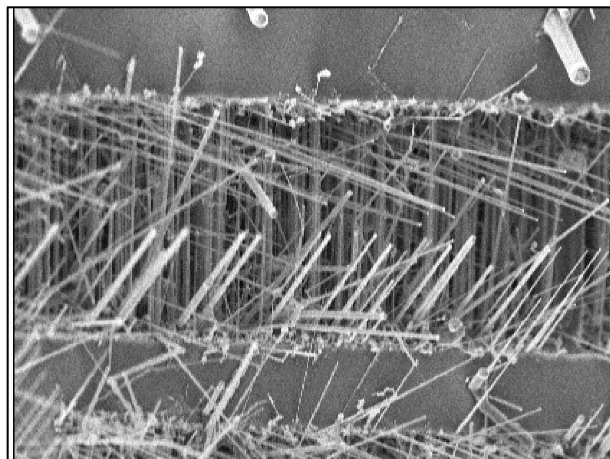
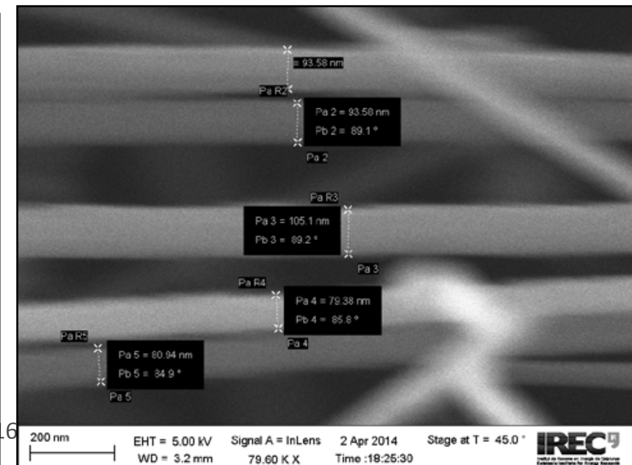
CVD-VLS – Nanowire control



- Growth rate increases with T
- Verticality has a maximum in 630 ºC
- Well aligned horizontal Si NWs were obtained in trenches





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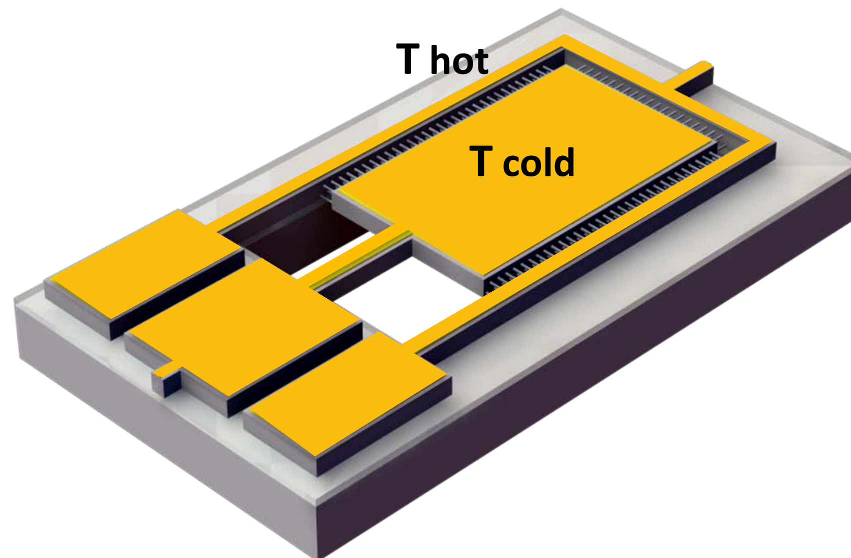
Bottom-up strategy – Device layout

Structural core will be a Si device micromachined in such a way that hot and cold areas develop when resting on a hot surface.

Hot area: surrounding rim **Cold area:** suspended platform.

Thermocouple: nanostructured silicon and thin metal film.



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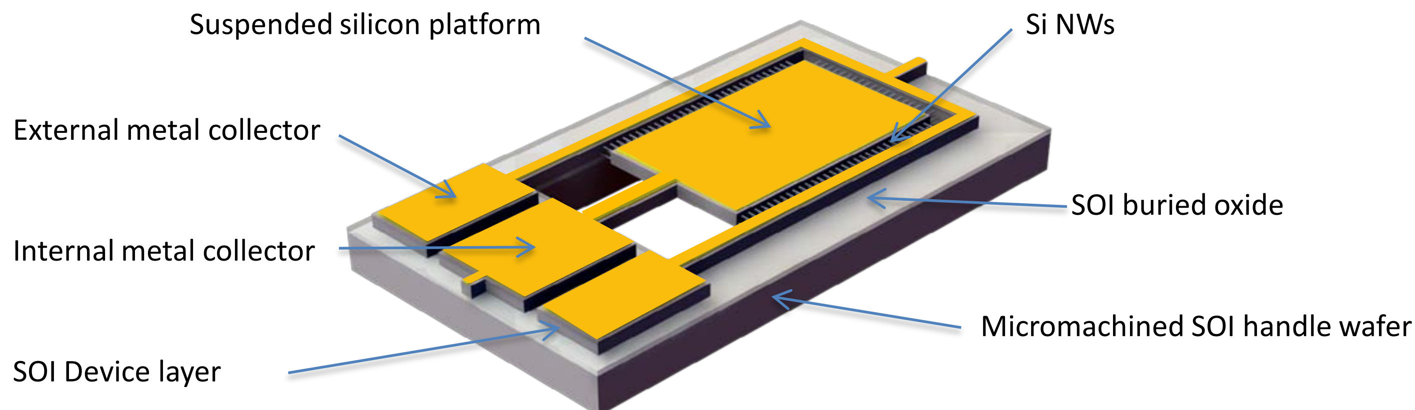
Bottom-up strategy – Device layout

- SOI wafers used as starting material. Device layer <110>, so that parallelograms with <111> oriented walls can be built .
- Typical size will be 1 mm, with 10 μm trench widths. Depth is fixed by device layer thickness, which will be around 10-15 μm to accommodate a large number of NWs.



Top-down strategy

NWs will be grown with a CVD method within nanometric cavities built up by controlled etching and filling of recessed regions (without nanolithographic steps).

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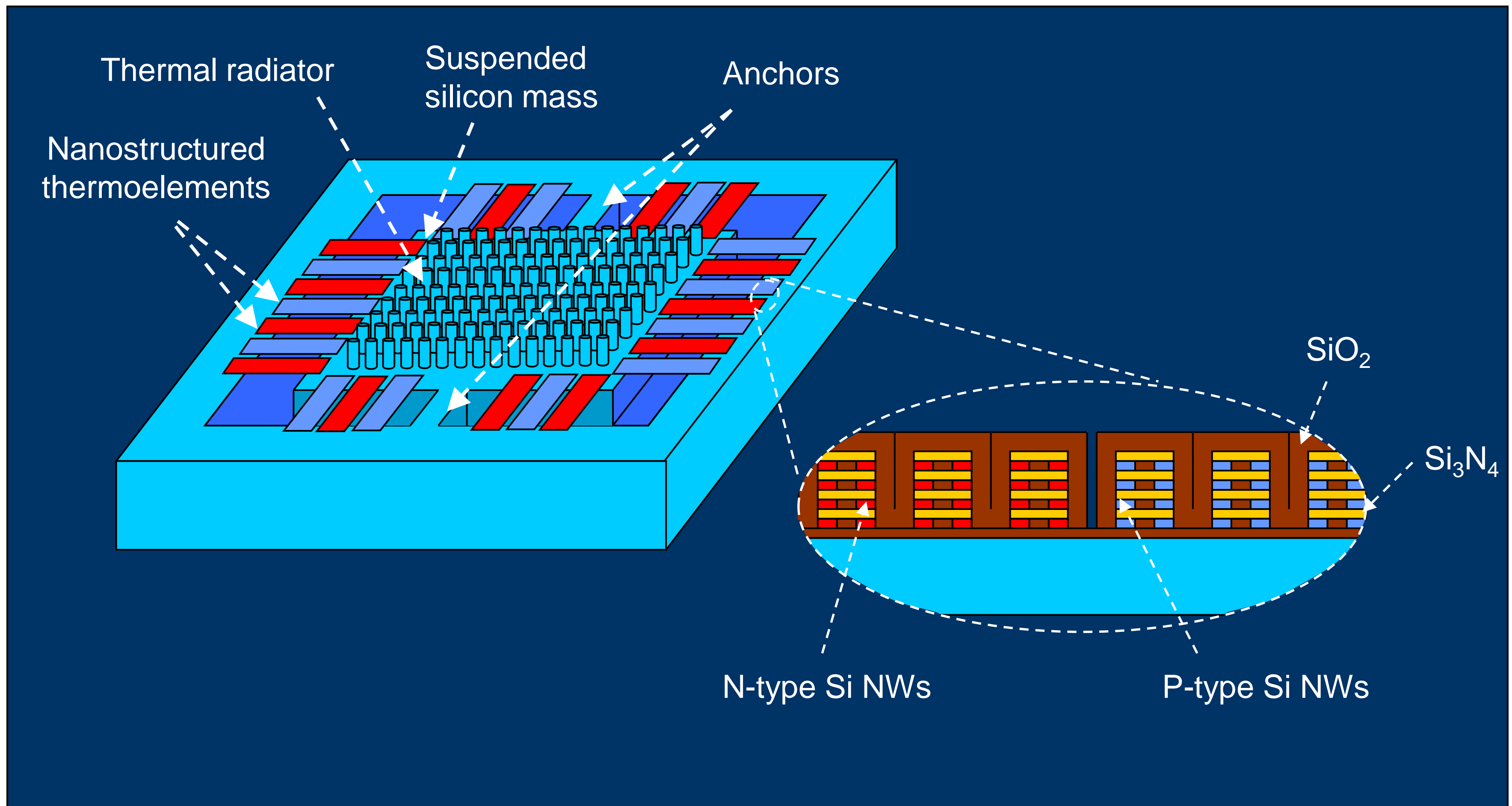
Top-down layout with lateral NWs:



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Top-down fabrication of lateral NWs:

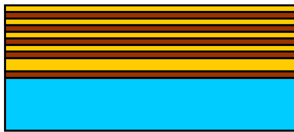
1. Si substrate

2. SiO_2 growth

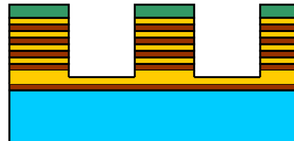
3. Si_3N_4 deposition

4. SiO_2 deposition

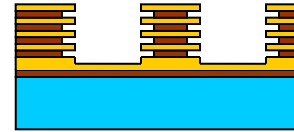
5. Si_3N_4/SiO_2 deposition



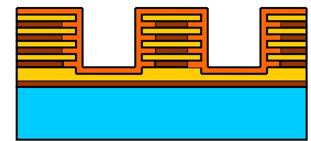
6. Si_3N_4/SiO_2 RIE



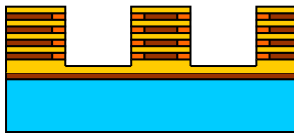
7. SiO_2 wet etching



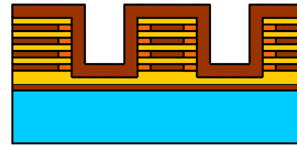
8. Poly deposition



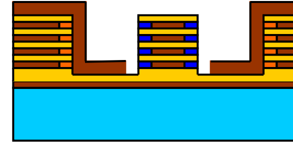
9. Poly etchback



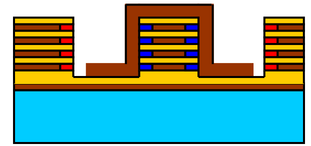
10. SiO_2 deposition



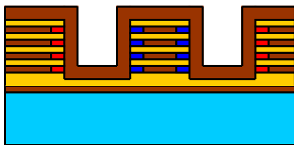
11. P-type doping



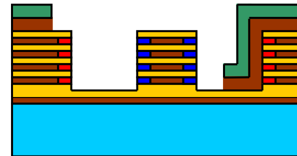
12. N-type doping



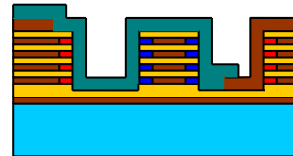
13. SiO_2 deposition



14. SiO_2 etching



15. Al patterning



Semicond. Sci. Technol. 26 (2011) 045005

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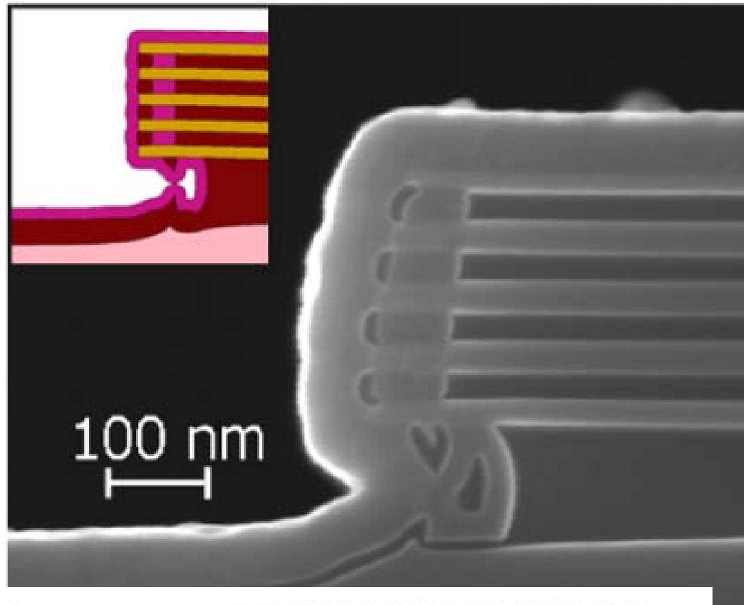
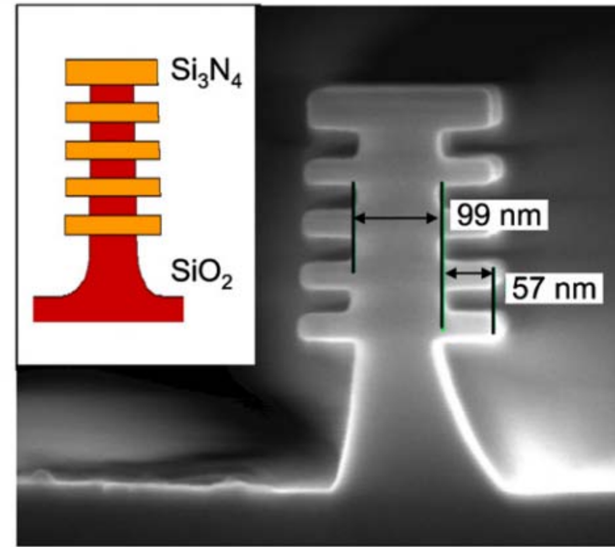




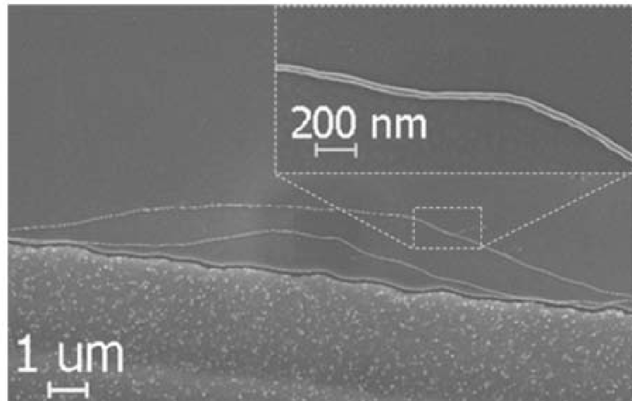
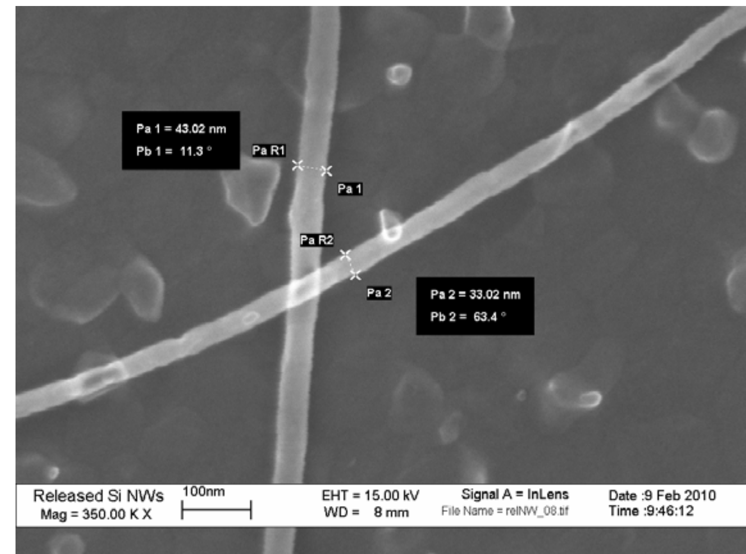


Fig. 5. SEM images at different magnifications of the nanowire after detachment from the hosting structure.



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From aims to practice

- NWs have high R_{th} (≈ 10^6 K $W^{-1}nm^{-1}$ /NW)
- For ΔT = 50 K, max heat acceptance is ≈ 25 pW/NW @ wire length of 1 mm
- If η = 5 % a target power output of 10 μW/cm^2 requires a wire density of 10^8 cm^{-2}, i.e. a wire spacing of about 1 μm

Critical design issues are:

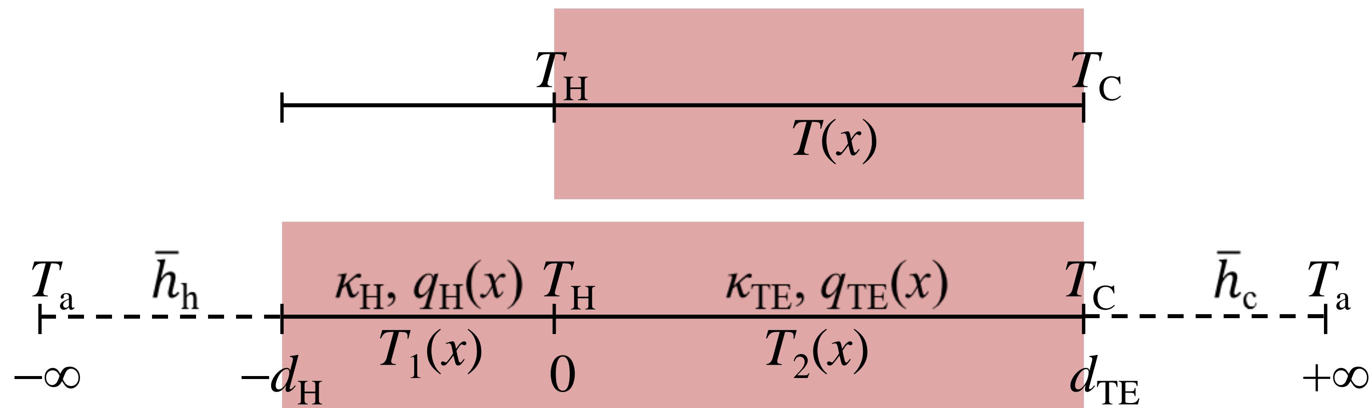
- optimal wire length
- optimal geometry (lateral or vertical)

The model

Choice of boundary conditions leads to contrasting design indications:

$$W_{el} = W_{th}\eta_{TE} = (\Delta T/R_{th})\eta_{TE}$$

- setting fixed-T BC's: W_{el} increases as R_{th} decreases
- setting fixed-heatflow BC's: W_{el} increases as R_{th} increases



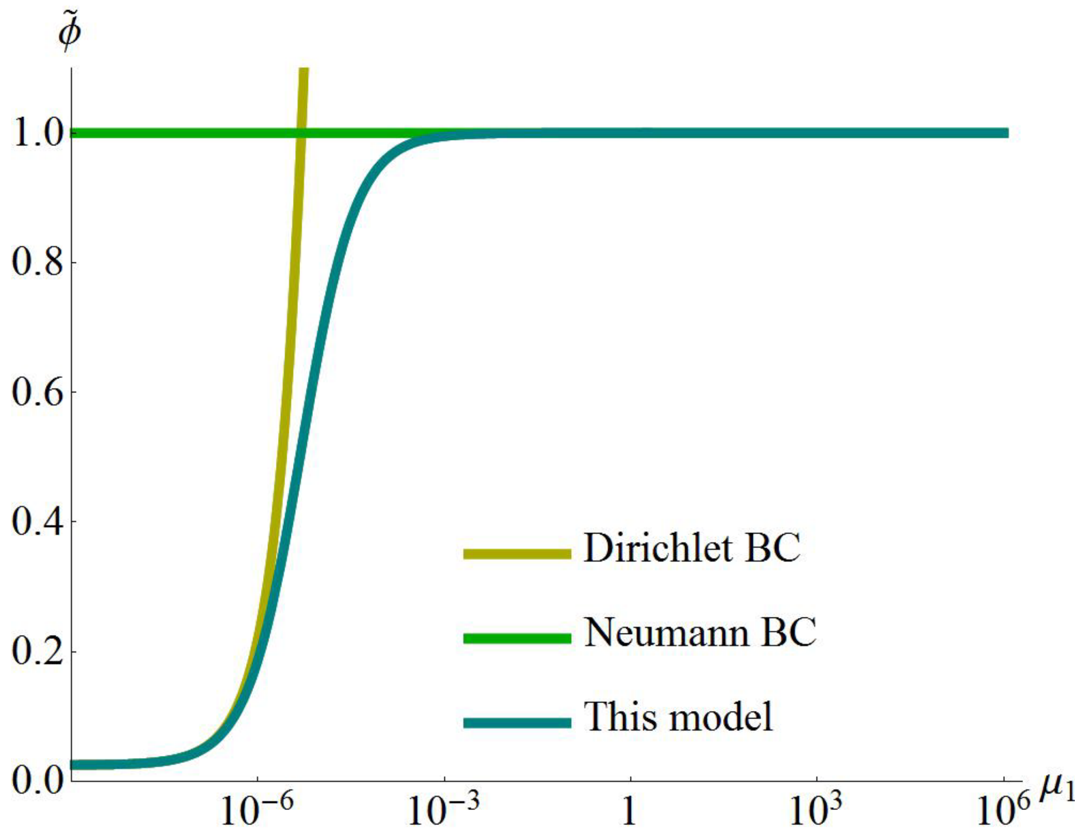
Model equation

$$
\begin{cases}
\kappa_{\mathrm{TE}} T_2''(x) + q_{\mathrm{TE}}(x) = 0 \\
\bar{h}_{\mathrm{c}}\left(T_2(d_{\mathrm{TE}}) - T_{\mathrm{A}}\right) = -\kappa_{\mathrm{TE}} T_2'(d_{\mathrm{TE}}) \\
\kappa_{\mathrm{H}} T_1''(x) + q_{\mathrm{H}}(x) = 0 \\
\bar{h}_{\mathrm{h}}\left(T_1(-d_{\mathrm{H}}) - T_{\mathrm{A}}\right) = \kappa_{\mathrm{H}} T_1'(-d_{\mathrm{H}}) \\
\kappa_{\mathrm{TE}} T_2'(0) = \kappa_{\mathrm{H}} T_1'(0) \\
T_1(0) = T_2(0)
\end{cases}
$$

$$
q_{\mathrm{H}}(x) \equiv \frac{\theta_{\mathrm{H}}}{d_{\mathrm{H}}} \Pi\left(\frac{x}{d_{\mathrm{H}}} + \frac{1}{2}\right) > 0
$$

$$
q_{\mathrm{TE}}(x) \equiv -\frac{\theta_{\mathrm{TE}}}{d_{\mathrm{TE}}} \Pi\left(\frac{x}{d_{\mathrm{TE}}} - \frac{1}{2}\right) < 0
$$

Reconciling with Neumann and Dirichlet



For ideally dissipating cold sides and perfectly insulated heat sources ($1/\mu_4 = \mu_5 = 0$) constant heat flow BCs are recovered for $\mu_1 > 1$ (Neumann)

$$\mu_1 \equiv d_{\mathrm{H}} / d_{\mathrm{TE}}$$

$$\tilde{\phi} \equiv \phi / \theta_{\mathrm{H}}$$

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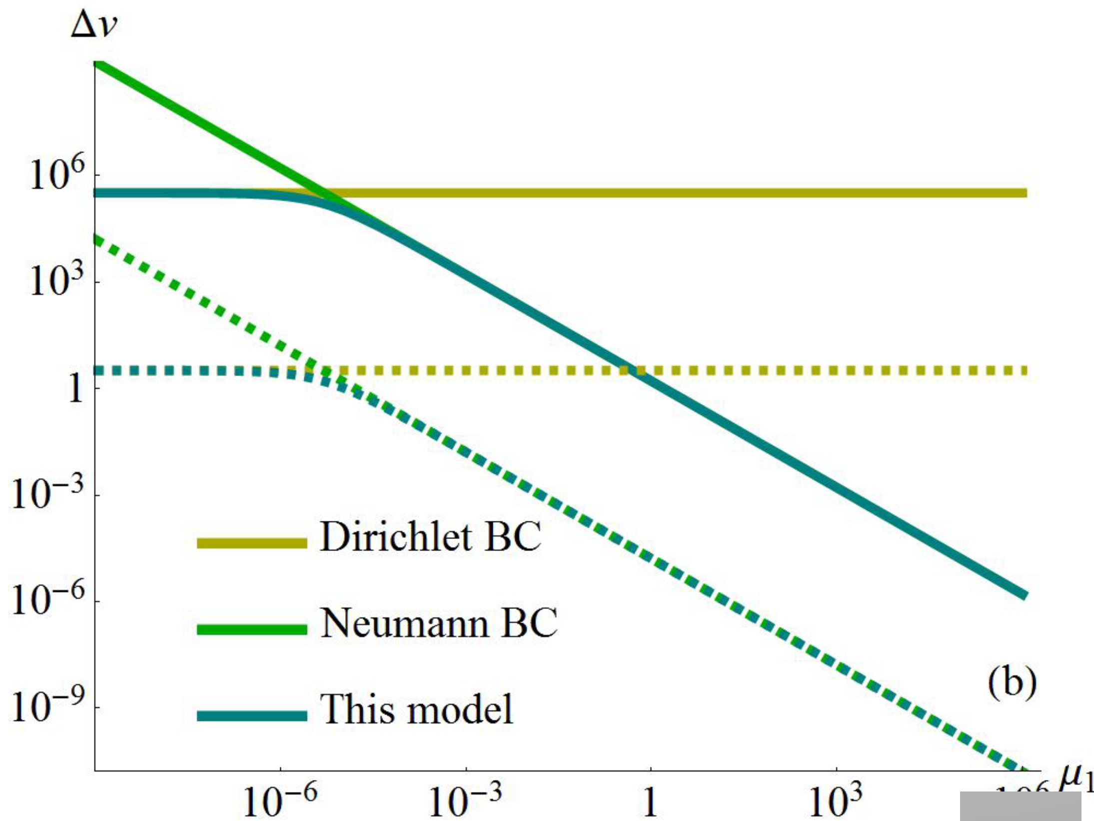
Reconciling with Neumann and Dirichlet



For ideally dissipating cold sides and perfectly insulated heat sources ($1/\mu_4 = \mu_5 = 0$) constant temperature BCs are recovered for μ_1<1 (Dirichlet)

Ideal dissipation conditions show that proper BCs switch upon d_H/d_{TE} ratio

$$\mu_1 \equiv d_H / d_{TE}$$

$$\Delta v \equiv v_H - v_C = (T_H - T_C) / T_a$$

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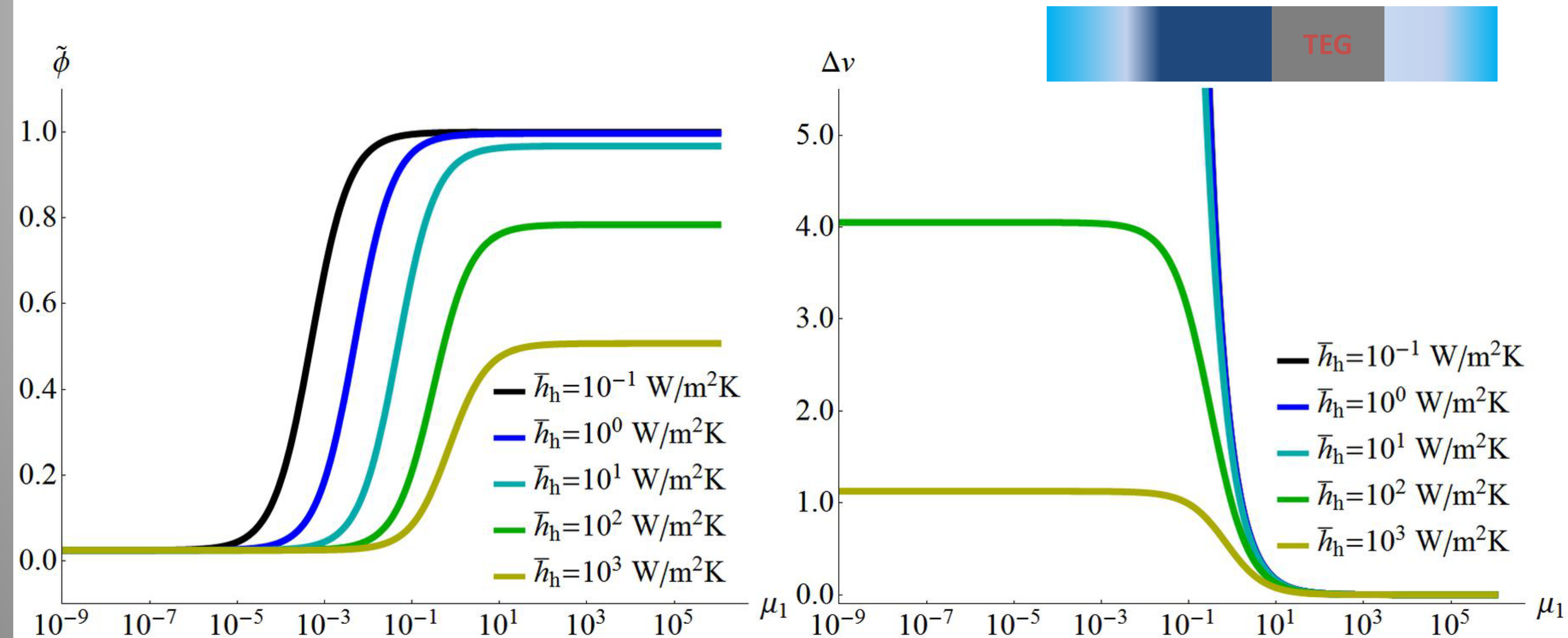
Dissipation efficiency



If the hot side is not perfectly insulated (or the heat source strength decreases) constant temperature/heat flow BCs do not apply around μ_1= 1. Since typical μ_1 for TEGs are between 10^{-1}- 10^{1} (bulk) and 10^{6} (micro/nano), application of standard analyses may mislead optimization of leg lengths.

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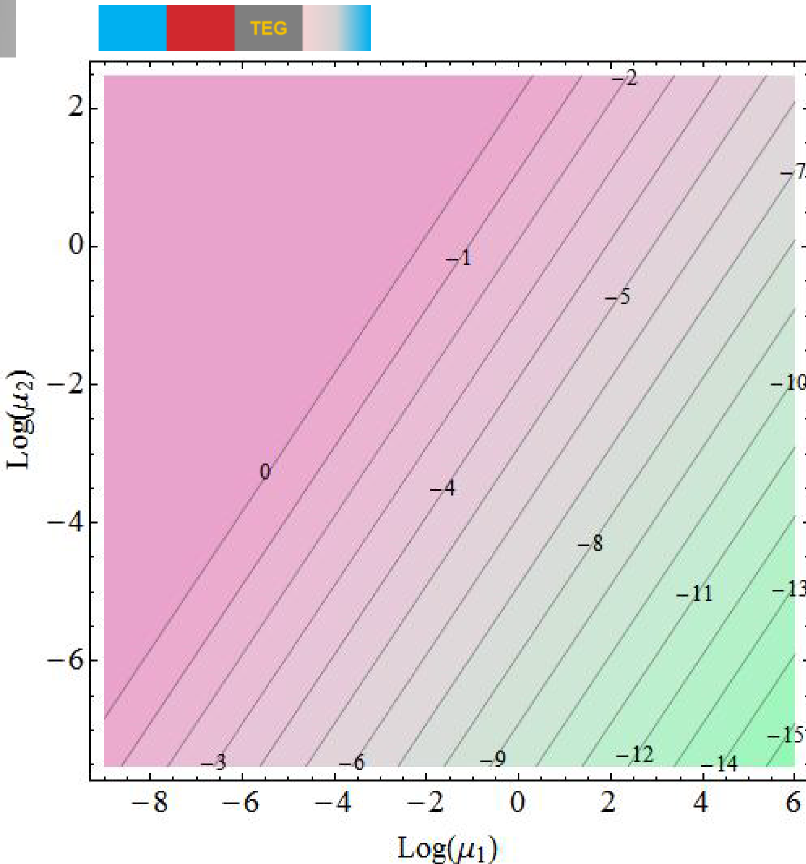
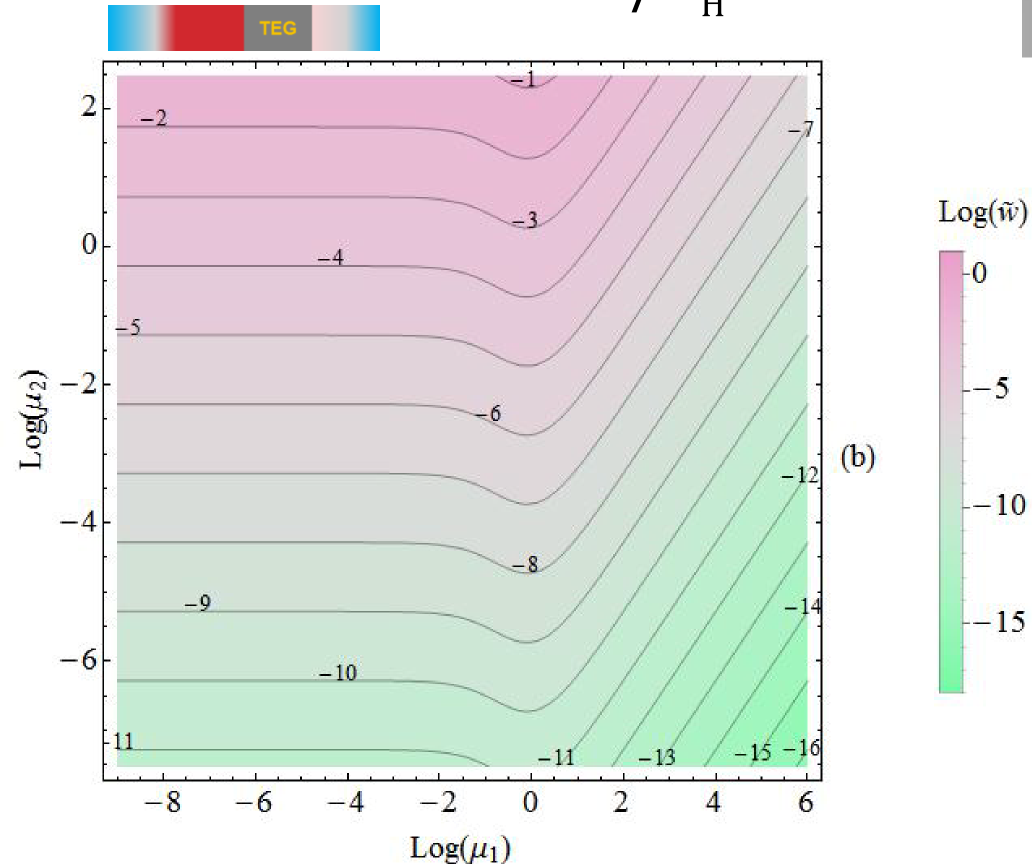
Power output

$$\mu_2 \equiv \theta_{\mathrm{H}} d_{\mathrm{H}} / (T_{\mathrm{a}} \kappa_{\mathrm{H}})$$

$$\tilde{w} \equiv w / \theta_{\mathrm{H}}$$





For sub-ideal hot side insulation or low heat source strength, power output remains constant in the $\mu_1 \rightarrow 0$ limit. Thus, TE legs should fulfill $\frac{d_{\mathrm{TE}}}{d_{\mathrm{H}}} < \mu_1^*$ (relevant for bulk TEGs).

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ZT, PF, κ, and leg lengths

The solution of the ODE's reads

$$v_i(\hat{x}) = \sum_{j=0}^{2} (\beta_{ji} / \beta_{\mathrm{D}}) \hat{x}^j \quad \text{with} \quad \beta_{ij} = \beta_{ij}(\ldots \mu_k \ldots)$$

$$\mu_1 \equiv d_{\mathrm{H}} / d_{\mathrm{TE}} \qquad \mu_2 \equiv \theta_{\mathrm{H}} d_{\mathrm{H}} / (T_{\mathrm{A}} \kappa_{\mathrm{H}}) = \theta_{\mathrm{H}} R_{\mathrm{H}} / T_{\mathrm{A}}$$

$$\mu_6 \equiv \kappa_{\mathrm{TE}} / \kappa_{\mathrm{H}} \qquad \mu_3 \equiv \theta_{\mathrm{TE}} d_{\mathrm{TE}} / (T_{\mathrm{A}} \kappa_{\mathrm{TE}}) = \theta_{\mathrm{TE}} R_{\mathrm{TE}} / T_{\mathrm{A}}$$

$$\mu_4 \equiv \kappa_{\mathrm{H}} / (d_{\mathrm{H}} \overline{h}_{\mathrm{h}}) = 1 / (R_{\mathrm{H}} \overline{h}_{\mathrm{h}}) \qquad \mu_5 \equiv \kappa_{\mathrm{TE}} / (d_{\mathrm{TE}} \overline{h}_{\mathrm{c}}) = 1 / (R_{\mathrm{TE}} \overline{h}_{\mathrm{c}})$$

Since κ's and d's enter the solution independently, the optimization of the TEG geometry will depend on material properties not only through ZT but also through PF and κ separately.

D. Narducci, J. Nanoeng. Nanomanuf. 1 (2011) 63−70.
D. Narducci, Appl. Phys. Lett. 99 (2011) 102104.

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Impact on the design of micro/nanoharvesters

- Dirichlet and Neumann solutions recovered for ideally dissipating systems
- When dissipation is less than ideal, deviations from simplified models may be relevant both for micro and macro-harvesters depending on the characteristics of the heat source (power strength and insulation toward the ambient)
- Expected power outputs are consistent with final device/application requirements (10 μW/cm^2)
- From the material scientist viewpoint, once again *ZT* and *κ* should be thought as interdependent parameters.

Summary

- Two redundant TEG strategies developed:
  - bottom-up, by VLS
  - top-down, by non-critical lithography
- Modeling set up to optimize wire lengths on the heat source
- All technologies are IC-compatible to support integration in the final prototype
- Technologies are flexible enough to be redeployed in other contexts

The WP2 Team

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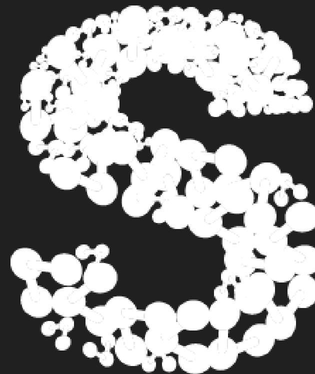

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